模拟集成电路课程设计（版图）
Layout in Analog Integrated Circuits

Assist. Prof. Jian Zhao
Prof. Guoxing Wang

Shanghai Jiao Tong University
School of Microelectronics
zhaojianycc@sjtu.edu.cn

Instructors

- **Time**
  - Lecture: Tuesday 14:00 to 15:00
  - Lab: Tuesday 15:00~17:30, Friday 14:00~17:30
- **Lecturer**
  - Assist. Prof. Jian Zhao (赵健) & Prof. Guoxing Wang
  - School of Microelectronics, Room 427
  - zhaojianycc@sjtu.edu.cn
- **Teaching Assistant**
  - Dr. Luo Jing (罗京)
  - School of Microelectronics, Room 404.
  - luojing@sjtu.edu.cn

Syllabus (New)

L1: Introduction & Active & Passive Components

L2: Process variation & Matching Issues

L3: Parasitic Effects

L4: ESD protection, Floorplan & Packaging

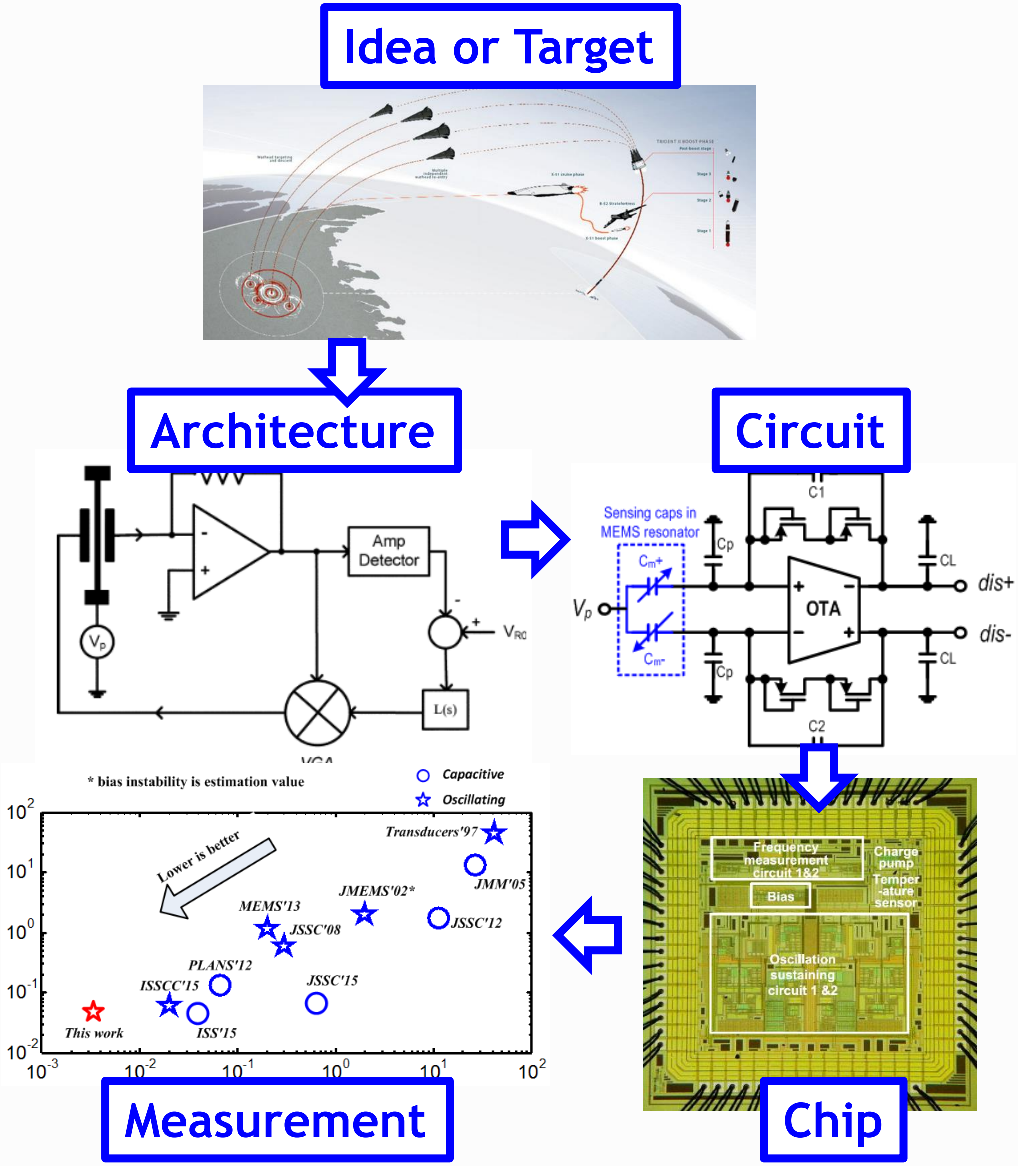
L5: Design for Manufacture (Prof. Li Yongfu)

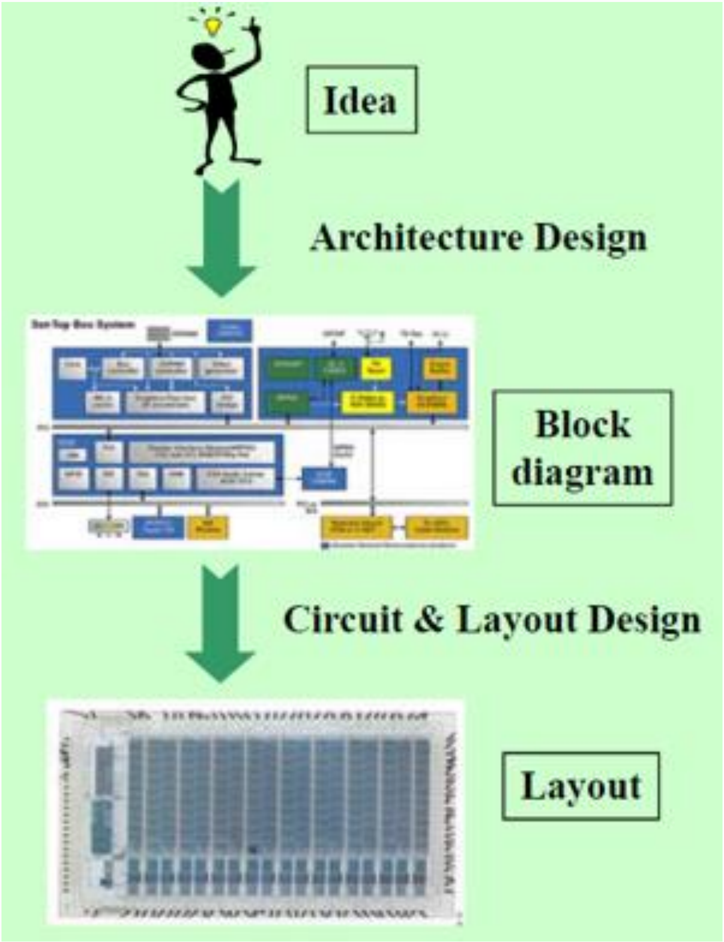
L6: Case Study: Design Flow of a Mixed Signal IC

L7: Miscellaneous (AMS tools, Auto Routing)

L8: Project Review

Introduction of Design Flow





Outline of Lecture #7

- Motivation
  - Case introduction, design flow
  - Motivation, Previous works review, benchmark
- Specification breakup & Block design
  - Modeling, Specification breakup
- Architecture & Circuit blocks
  - Architecture & key technology, circuit blocks
- Chip implementation
  - Auxiliary circuit & whole chip layout
- Measurement

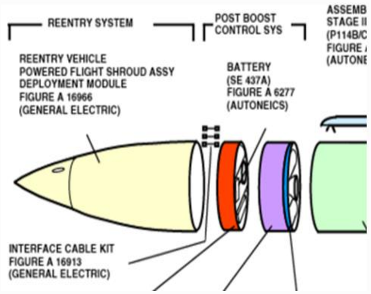
Introduction

- Navigation is necessary in different area **PNT Issue!!!**
- Applications
  - （GPS permitted）
  - Vehicle
  - Mobile Devices

MEMS Sensors, great success!

  - （GPS denial）
  - Smart Ammunition, UAV (in some cases)
  - Indoor/underground Navi.

Traditional Sensors meet the requirement !



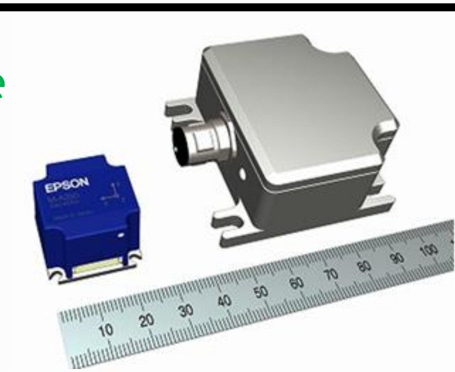
Introduction

- Conventional Sensors, MEMS Sensors

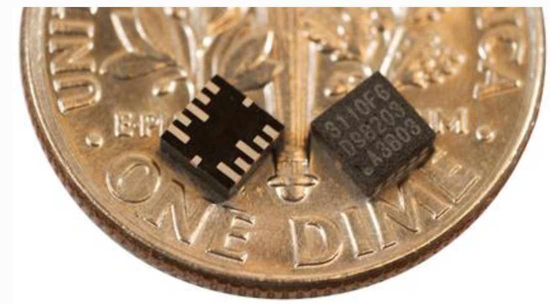
VBA

Mechanical Servo Accelerometer

√ Good performance
X large size
X poor reliability
X high power
X high cost



MEMS Accelerometer



X poor performance
√ small size
√ good reliability
√ low power
√ low cost

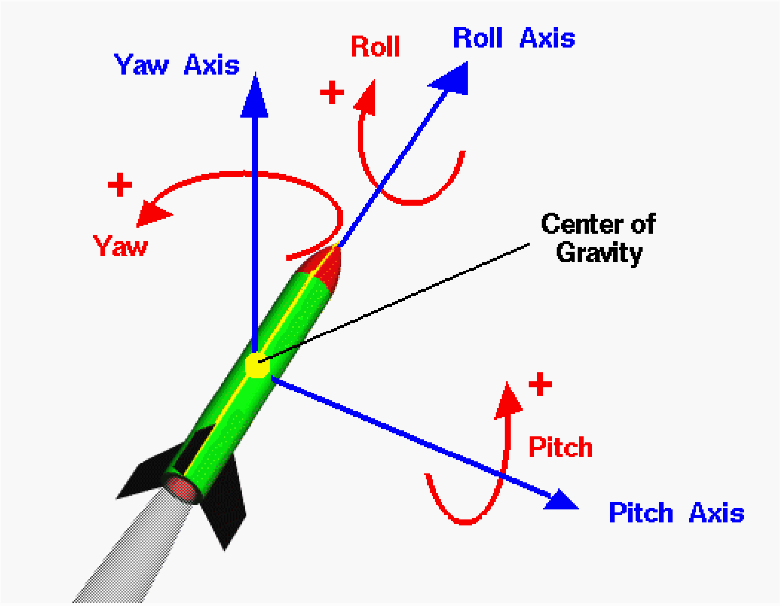
CMOS compatible

Navigation is too expensive! MEMS sensors are still not applicable!

Introduction

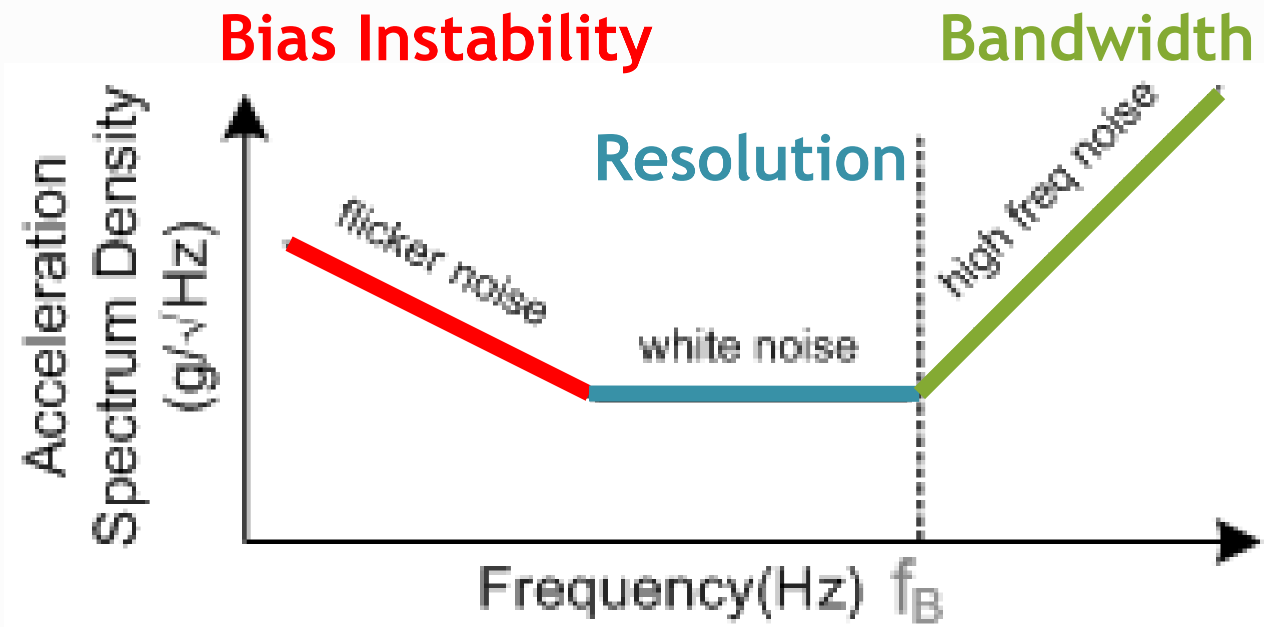
- Inertial Navigation & Required Performance
  - 3 Axis Accelerometer: relative motion
  - 3 Axis Gyroscope: attitude
  - Other Sensor: redundant correction

navigation algorithm
Absolute position



Specifications

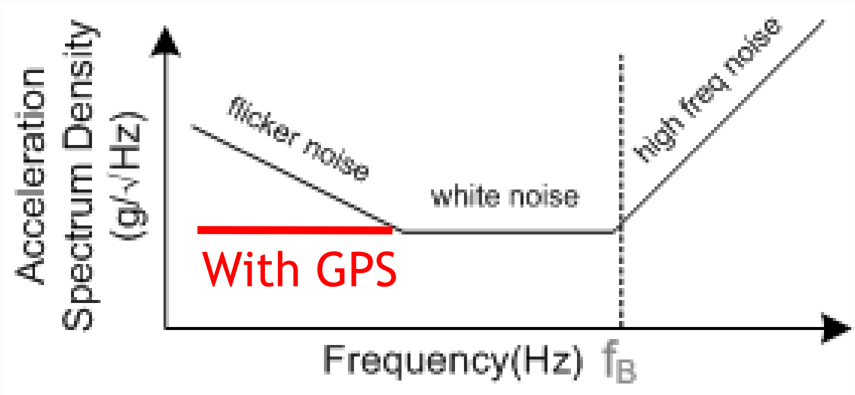
- Why Not GPS?
  - Bandwidth of GPS is limited (max:15Hz)
  - Operates in highly contested theaters
- How to evaluate the accelerometer?

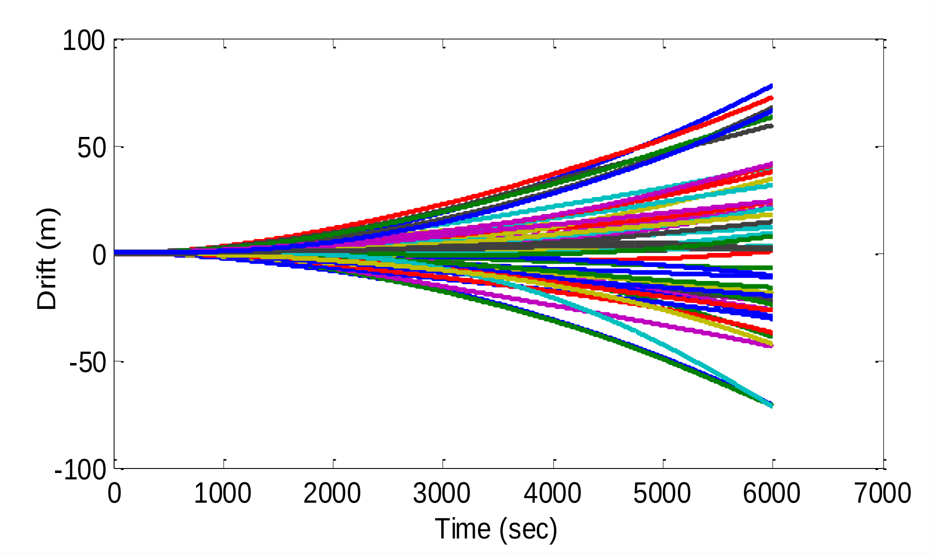


Introduction

- Why Not GPS?
  – Bandwidth of GPS is limited (max:15Hz)
  – Operates in highly contested theaters
- Who contributes to CEP? Challenge!

$$d(t) = \iint_{0\to T} a(t)\,\mathrm{dt}$$

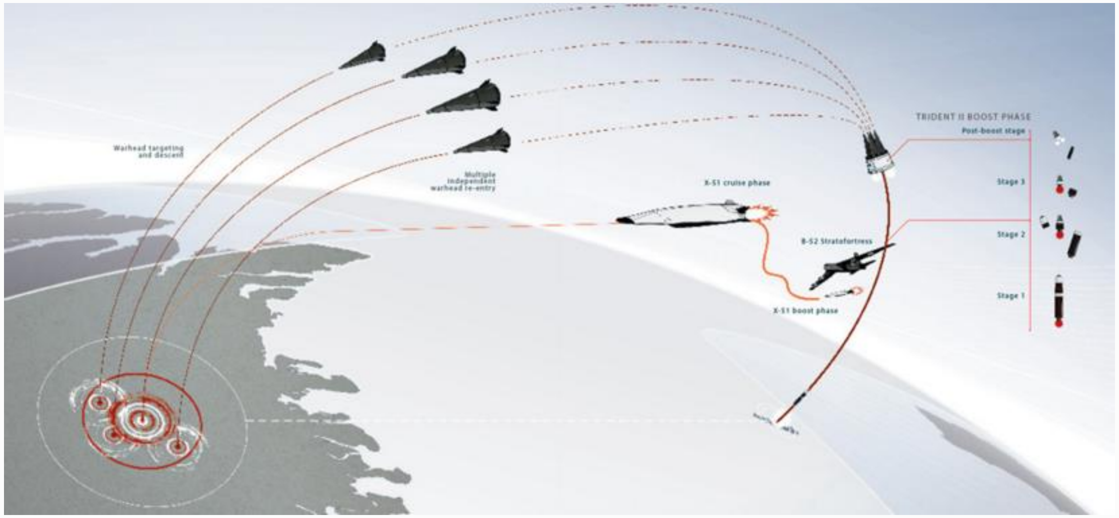


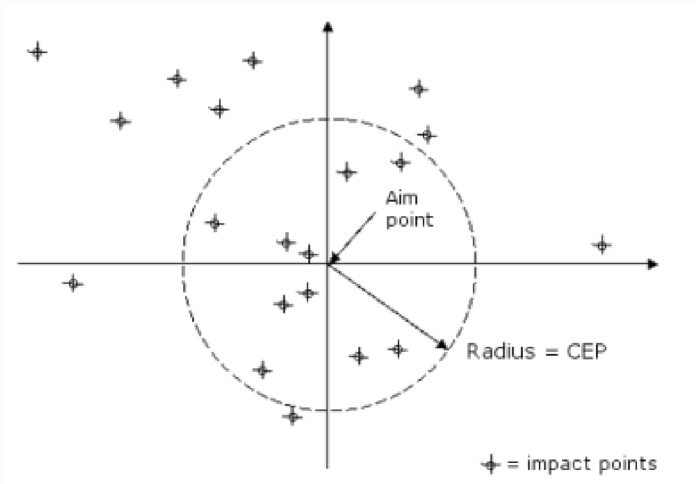


Drifts under 1μg@1Hz flicker noise level

Introduction

- Inertial Navigation
  - Circular Error Probable (CEP)

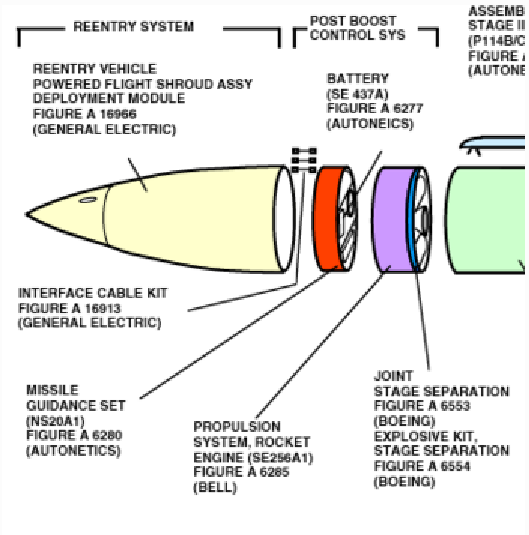




Accuracy measure	Probability (%)
Root mean square (RMS)	63 to 68
Circular error probability (CEP)	50
Twice the distance root mean square (2DRMS)	95 to 98
95% radius (R95)	95

Introduction

- Typical Ballistic Missile and their CEPs



Model	Range(km)	CEP(m)
LGM-30	13k	200
Trident missile	7.4k	450
Trident missile II	12k	90
LGM-118A	14k	90
PT-2ПМ2	>12k	<110
DF-5	14k	800
GPS	Unlimited	5

Duration:
1200~1800sec
Requirement:
<0.1 μg instability

Literature review

- Comprehensive review related works

Type	Year	MEMS proc.	Noise floor	Bias instab.	BW	SF	Full Scale	Power	Readout	Reference	Affiliation
		μm	μg/√Hz	μg	Hz	Hz/g	±g	mW			
Capacitive	2002	6	2		1000		0.125		CMOS-0.8, OL, SC	Jiang SSA&M 2002	UCBerkeley
	2006	70	2.7		100		1	12	CMOS OL/CL SDM	Chae, JMS 2005	U Michigan
	2006	70	1.08				1.35	7.2	CMOS-0.5, OL SDM FE	Kulah, JSSC 2006	U Michigan
	2006	40	4	2	100			4.5	CMOS-0.5, CL, 4th-order SDM	Amini, JSSC 2006	GIT
	2008		704				2	0.0015	CMOS-0.25, OL, SC SDM	Kamarainen, ISSCC 2008	Helsinki UT
	2009		482				4		BiCMOS-0.13, OL, CT	Paavola, JSSC 2009	Helsinki UT
	2009		7.1		300			12	CMOS+FPGA, CL, hybrid 5th-order SDM	Zwahlen, ESSCIRC 2009	Colibrys
	2010		45	31	400		9.4	0.17	CMOS-0.13, OL, CT FE only	Bernal, EMBS 2010	IME, A*Star
	2011		15		100		2.5	0.015	CMOS-0.25, FE only	Santana, Transducer 2011	IMEC/MEMSCAP
	2011		25				11.5	1	CMOS-0.35, OL, CT, FE only	Sun, Sensor J 2011	U Florida
	2012		2	1	1000		15	100	CMOS+FPGA, CL, hybrid 5th-order SDM	Zwahlen, PLAN 2012	Colibrys
	2013		220		200		9.14	3.1	CMOS-0.18, CL SDM,	Lajevardi JSSC 2013	Bosch/Stanford
	2014		25.5	15	1000		1-100	10	CMOS, OL	Rudolf, PLAN 2014	Colibrys
	2015		0.2	18	300		1.2	23	CMOS-0.5, CL, 5th-order SDM	Xu, JSSC 2015	HIT, China
	2015		1.16	7.5	250		1.25	1.2	CMOS-0.35, OL, SC	Wang, Sensor J. 2015	NTU, Singapore
SOA	2008	20	20	4		140	20	23	CMOS-0.35, SC	He, JSSC 2008	NUS, Singapore
	2012	15	360	2000		126		0.022	CMOS-0.15, Pierce Osc.	Tocchio, 2012	Politecnico di Milano
	2014		111	223	100		8	0.115	Discrete, Piezoresistive	Langfelder, TIE 2014	Politecnico di Milano
	2015	**80**	**2**	**0.6**	**10**	**140**	**20**	**3.5**	**CMOS-0.35, CT**	**Zhao, JSSC 2015**	**NUS, Singapore**
	2015	**80**	**1.2**	**0.4**	**10**	**140**	**20**	**4.7**	**CMOS-0.35, CT**	**Wang, ISSCC2015, JSSC 2017**	**NUS, Singapore**
	2016	**80**	**1.6**	**0.23**	**10**	**140**	**30**	**2.7**	**CMOS-0.35, CT**	**Zhao, VLSI2016, JSSC 2017**	**NUS, Singapore**
	2017	**60**	**0.38**	**0.095**	**250**	**224**	**15**		**Discrete**	**Yin, S&A A, 268, 2017**	**Tsinghua, China**
FM	2012	100	25	5		4			Discrete, 4xMass,	Trusov, PLAN 2012	UCIrvine
	2013	100		6		4.4	20		Discrete, 4xMass,	Trusov, MEMS 2013	UCIrvine

http://www.yongpingxu.com/inertial-sensor-survey.html

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- Comprehensive review related works

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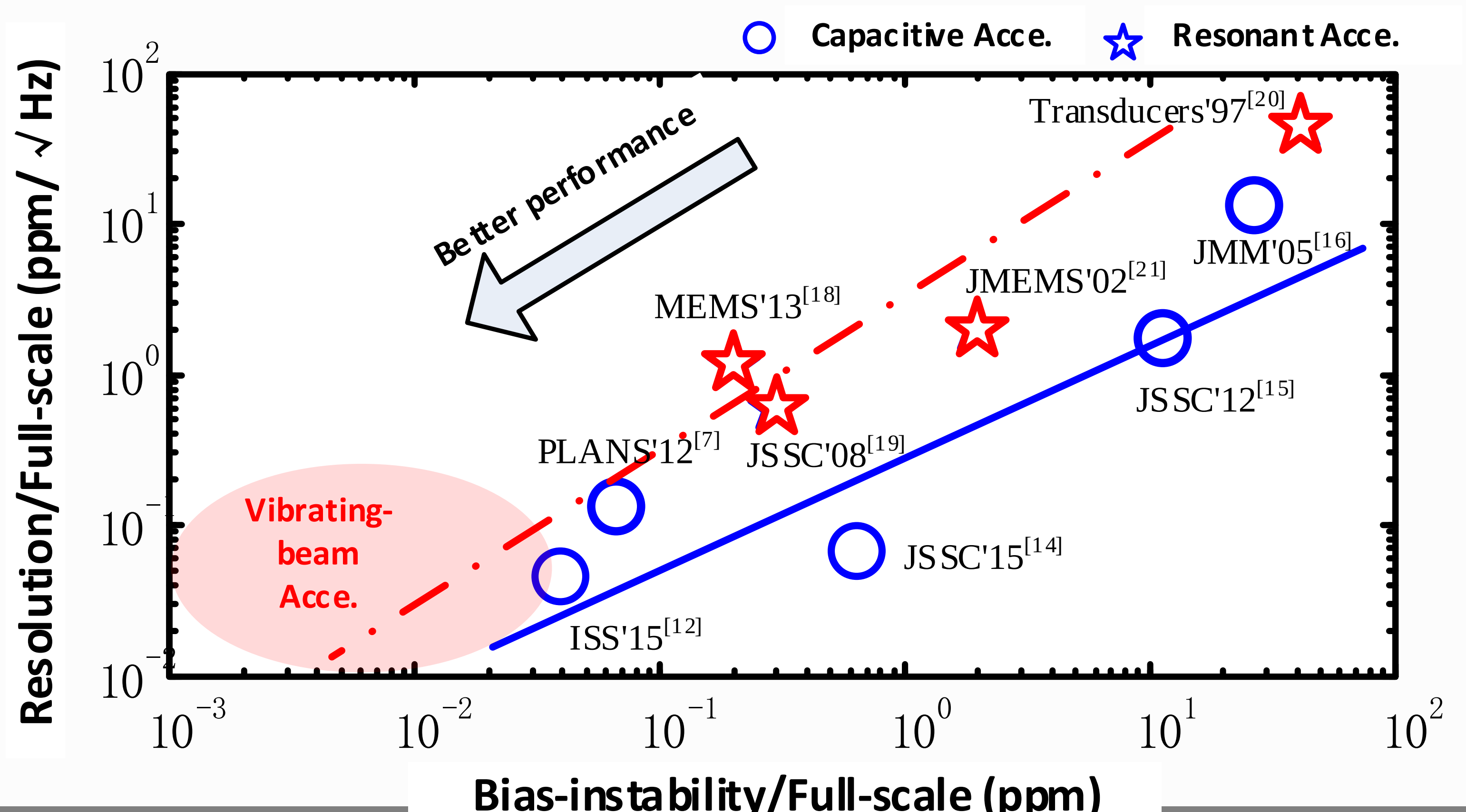
Industry

http://www.yongpingxu.com/inertial-sensor-survey.html

Literature review

- Comprehensive review related works
- Insightful summarization
  - A. "Moore's law" B. Gap between tech. and app.



Summary

- 1. Miniaturized sensor with high performance is an active research topic.
  - Both academic and industry are involved in it recent years
- 2. Long-term stability still have gap from application.
- 3. Trend tells us, we still have chance to shorten or eliminate the gap.

Two key issues during CHIP definition:

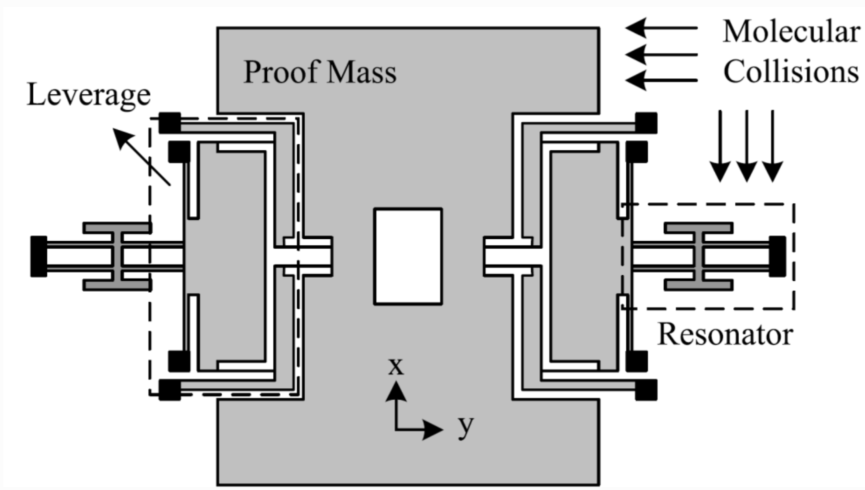
Significance! & Feasibility!

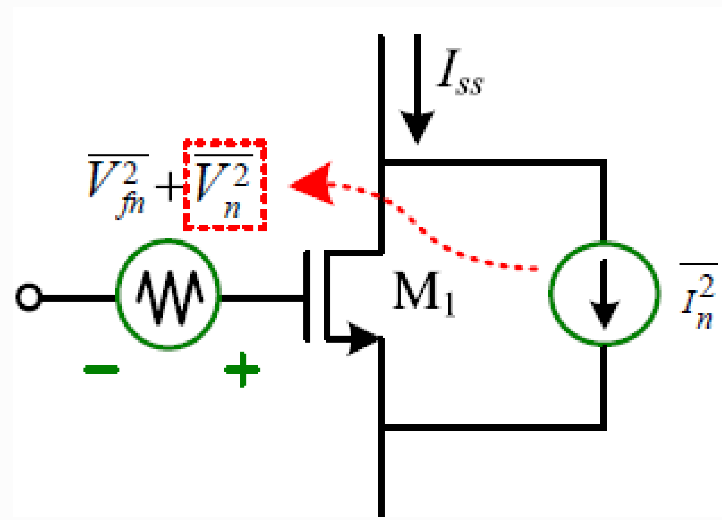
Outline of Lecture #7

- Motivation
  - Case introduction, design flow
  - Motivation, Previous works review, benchmark
- Specification breakup & Block design
  - Modeling, Specification breakup
- Architecture & Circuit blocks
  - Architecture & key technology, circuit blocks
- Chip implementation
  - Auxiliary circuit & whole chip layout
- Measurement

Noise Sources

- Noise classification by noise source
  - **Mechanical Noise:** Random collisions on resonator or proof mass (only white noise)
  - **Electronic Noise:** MOSFET, resistor etc. (white noise and flicker 1/f noise)

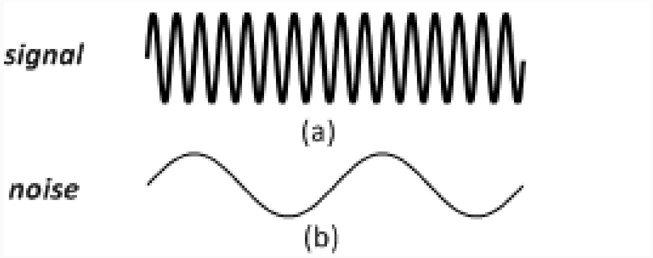


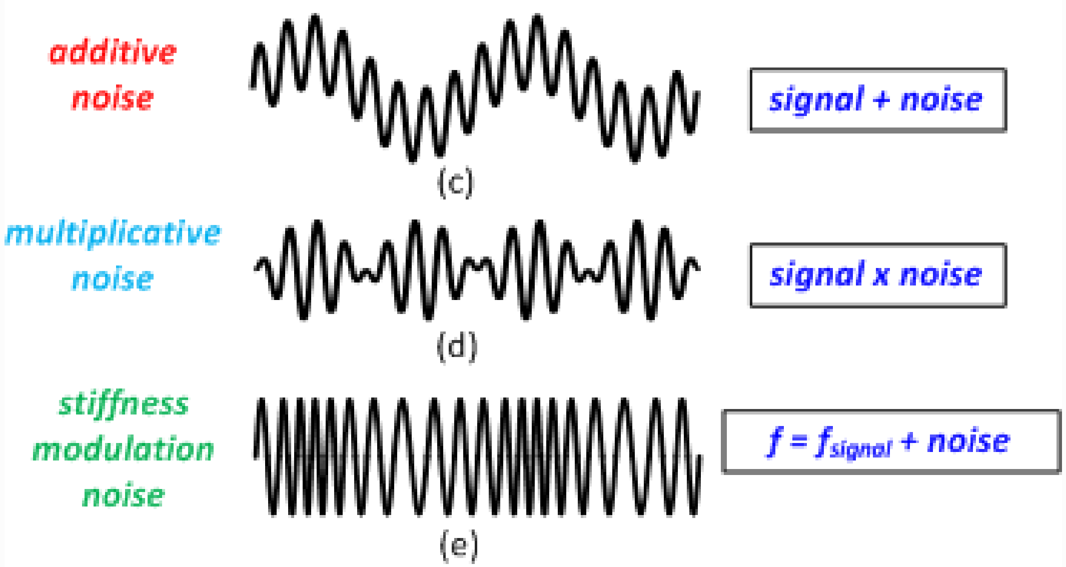


Noise Classification

- Classification by noise perturbation
  - Additive noise
  - Multiplicative noise
  - Stiffness modulation noise

} Parameter variation (LTV)





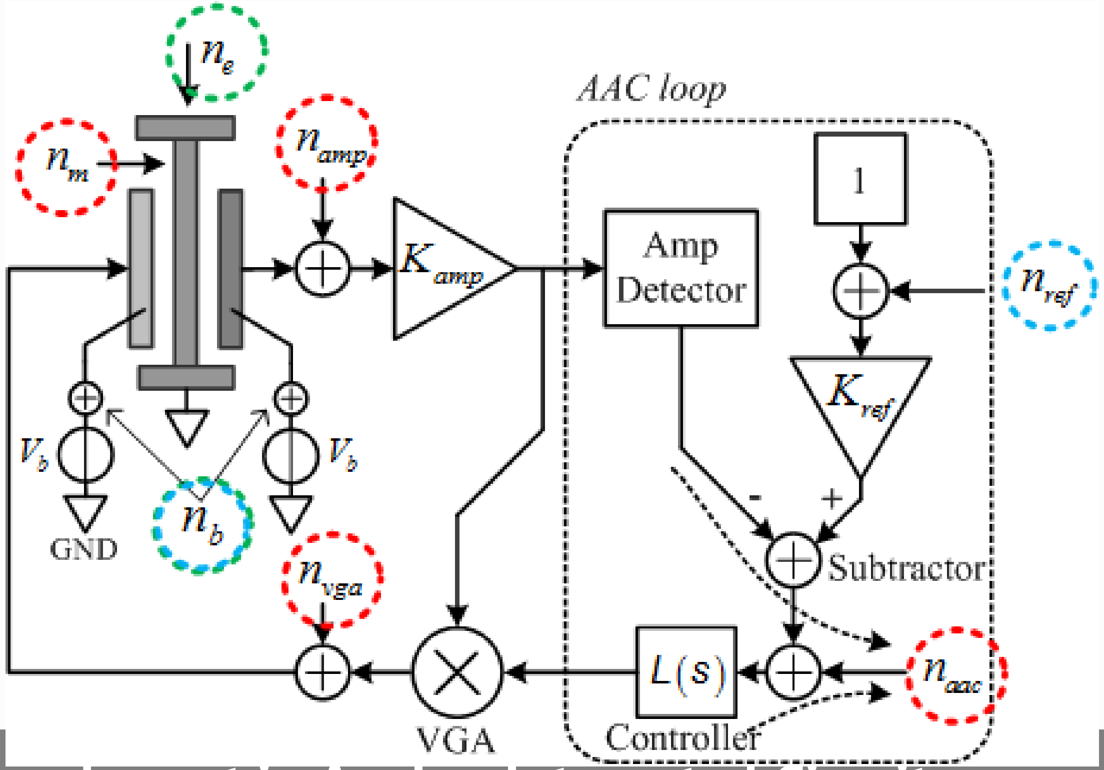
Ideal oscillation & Noise

Perturbed oscillation

Noise Classification

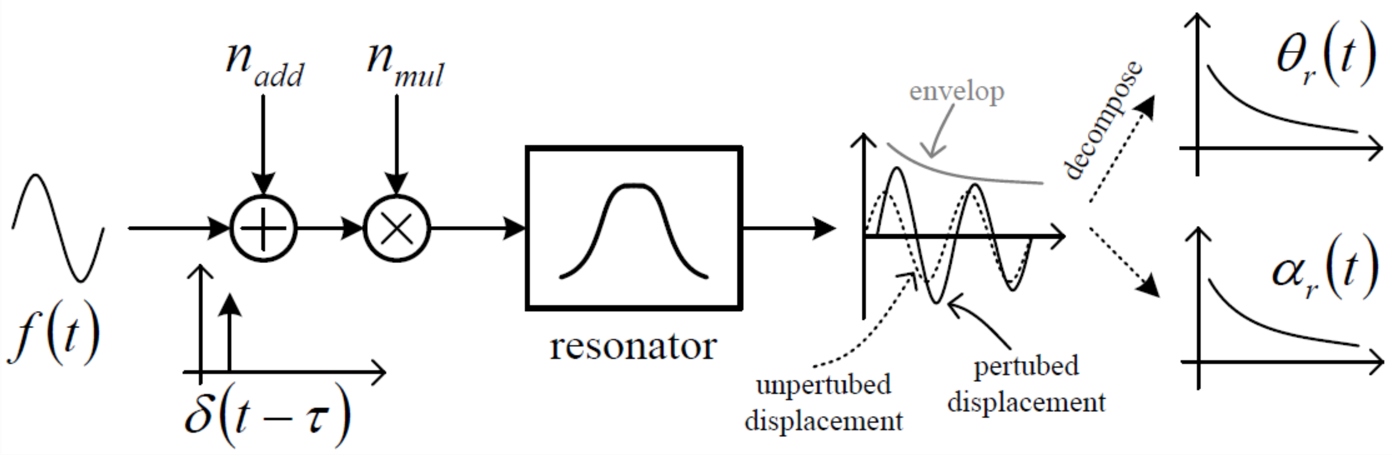
- Classification by noise perturbation
  - Additive noise (n_m, n_{amp}, n_{vga}, n_{aac})
  - Multiplicative noise (n_b, n_{ref})
  - Stiffness modulation noise (n_b, n_e)

} Parameter variations (LTV)

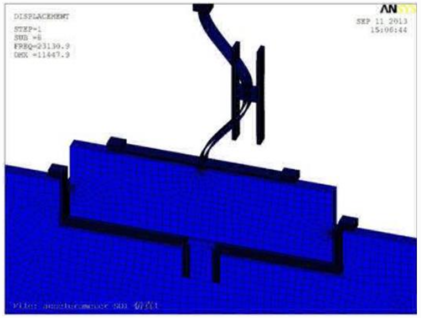


Noise Responses Analysis

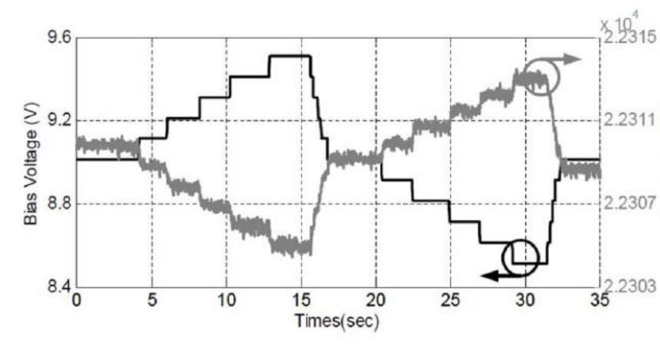
- Responses of Additive and Multiplicative noise



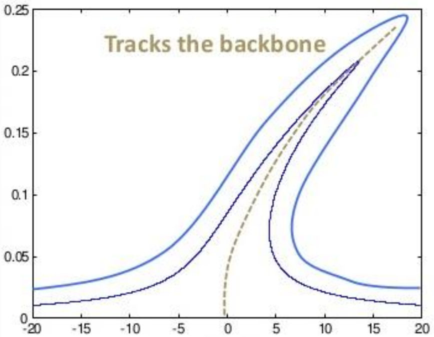
- Responses of stiffness modulation noise



Mechanical Modulation



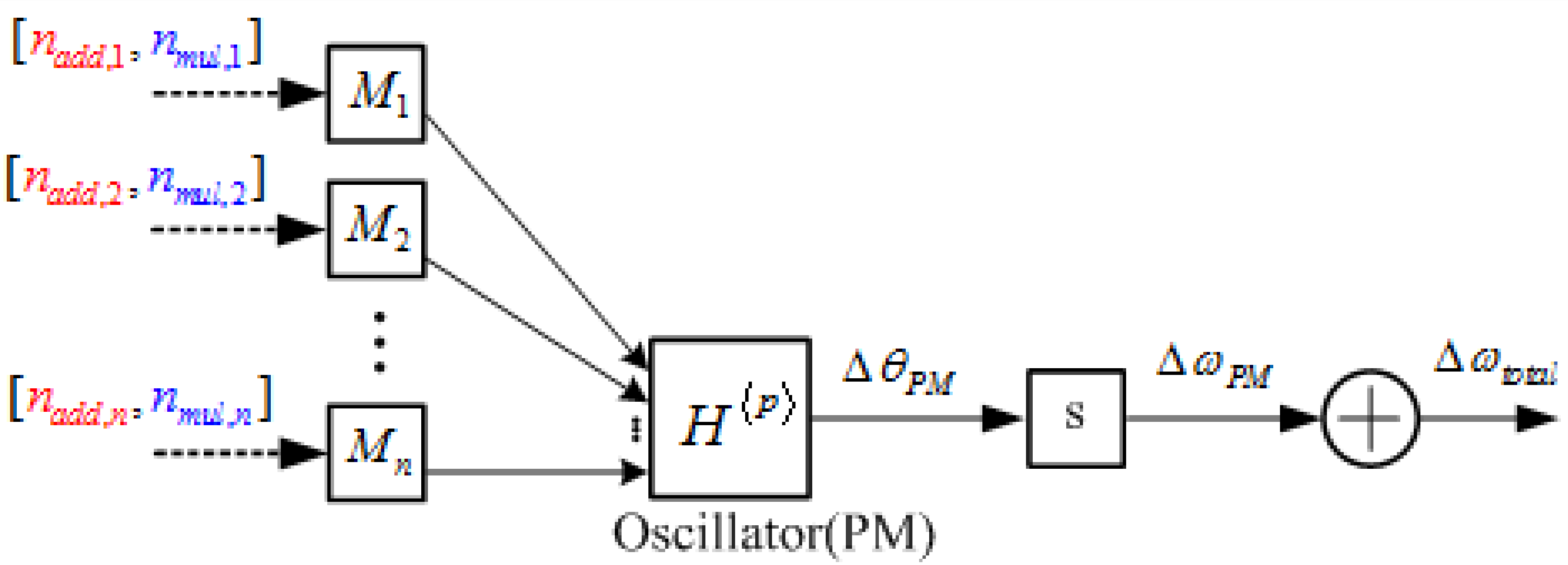
Electro-static Modulation



Amplitude Modulation

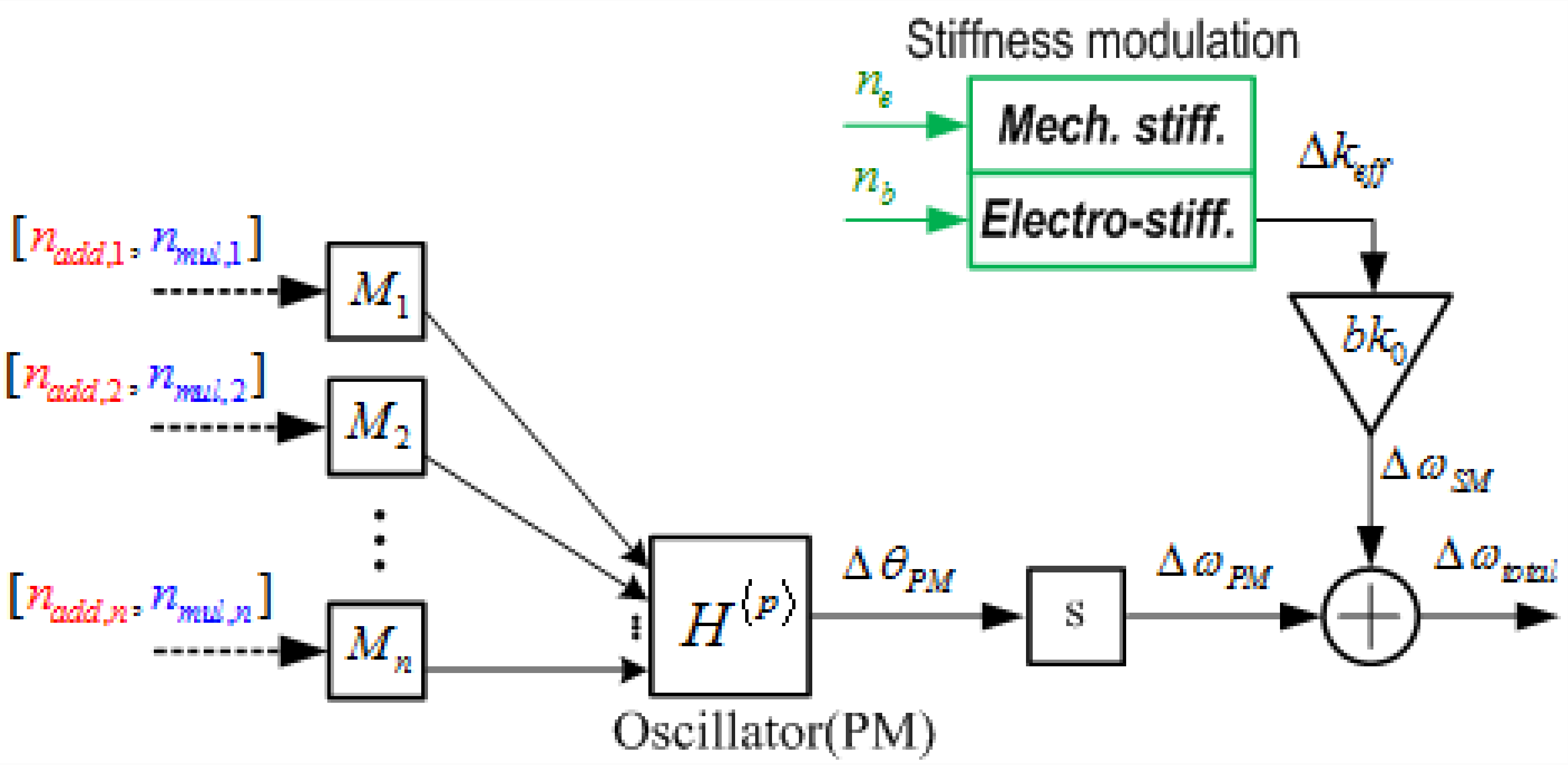
Entire Phase Noise Model

- **<u>Conventional phase noise:</u>** additive and multiplicative noise in oscillator introduce phase noise



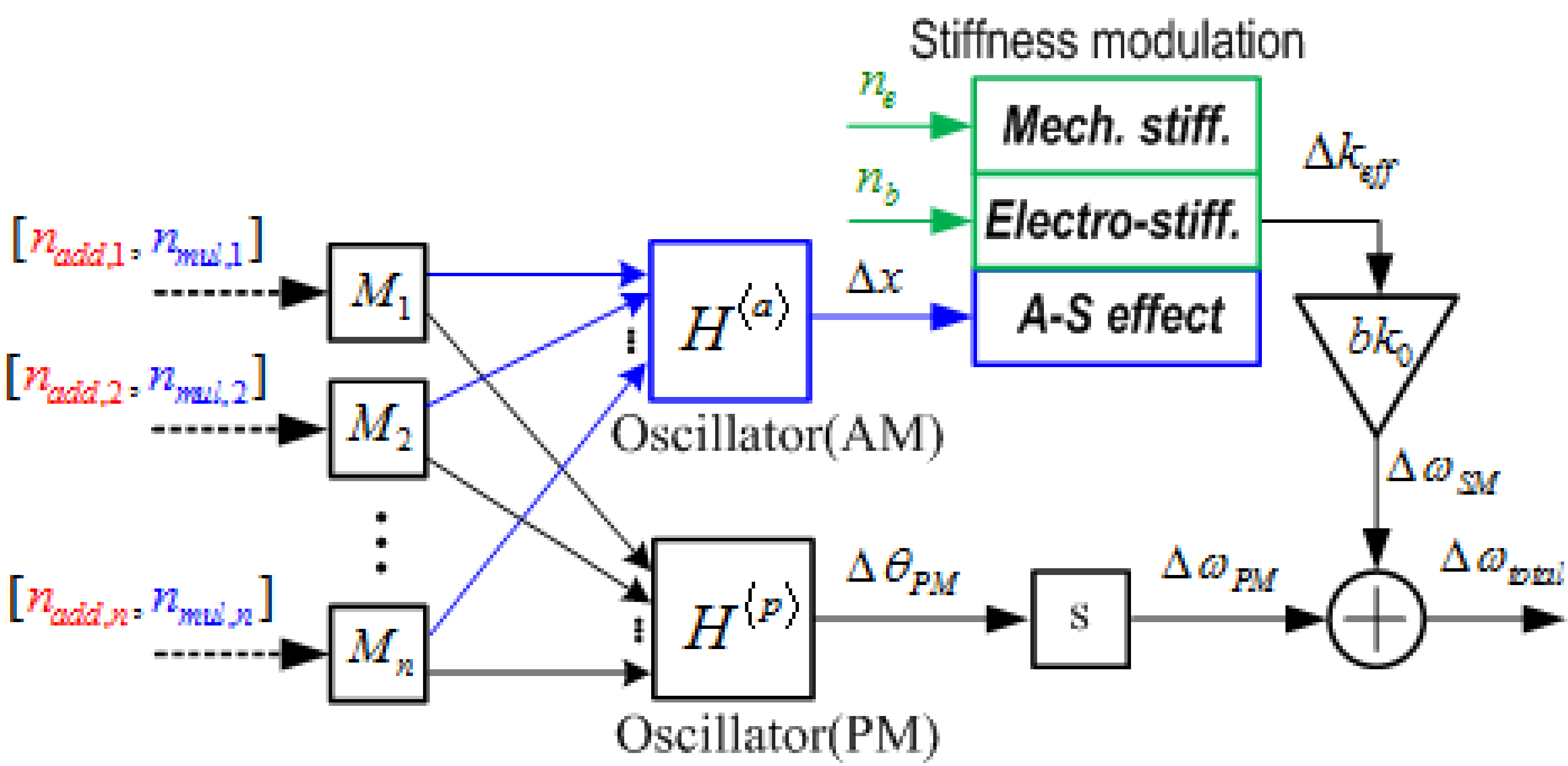
Entire Phase Noise Model

- **Stiffness modulation:** stiffness modulation noise directly change the oscillation frequency



Entire Phase Noise Model

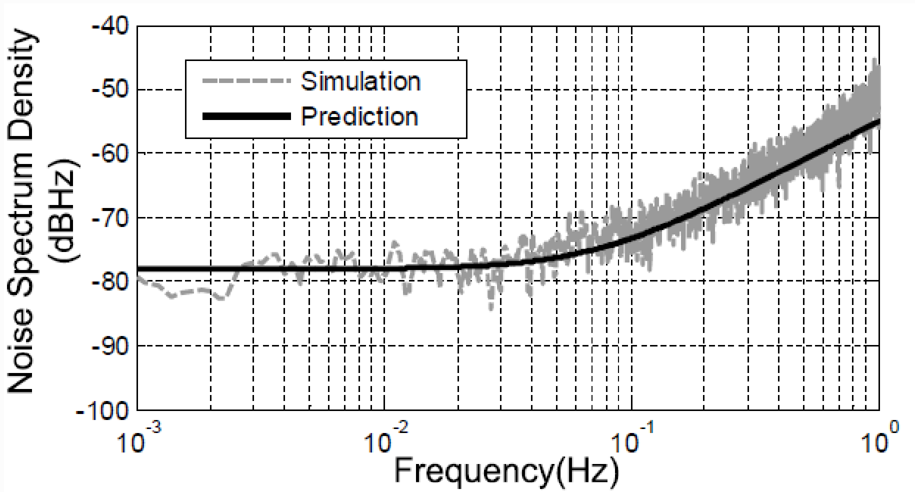
- **A-S effect:** nonlinearity in MEMS resonator introduces a coupling path between **amplitude** and **frequency**



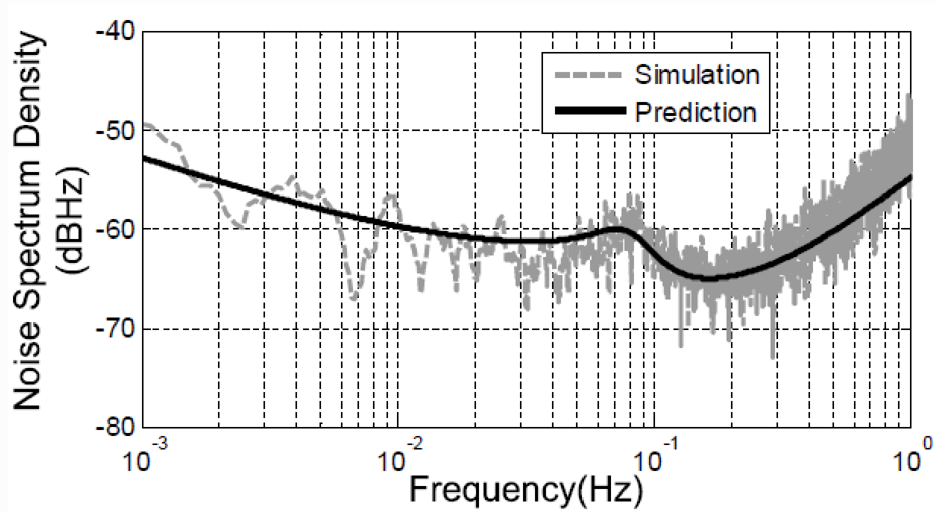
Noise prediction vs. trans. Sim.

- **<u>Nonlinearity turned off:</u>** flicker noise do not influence the oscillation frequency
- **<u>Nonlinearity turned on:</u>** flicker noise disturbs the oscillation frequency through stiffness modulations

Flicker noise stem from amplitude, amplified by nonlinearity!!!



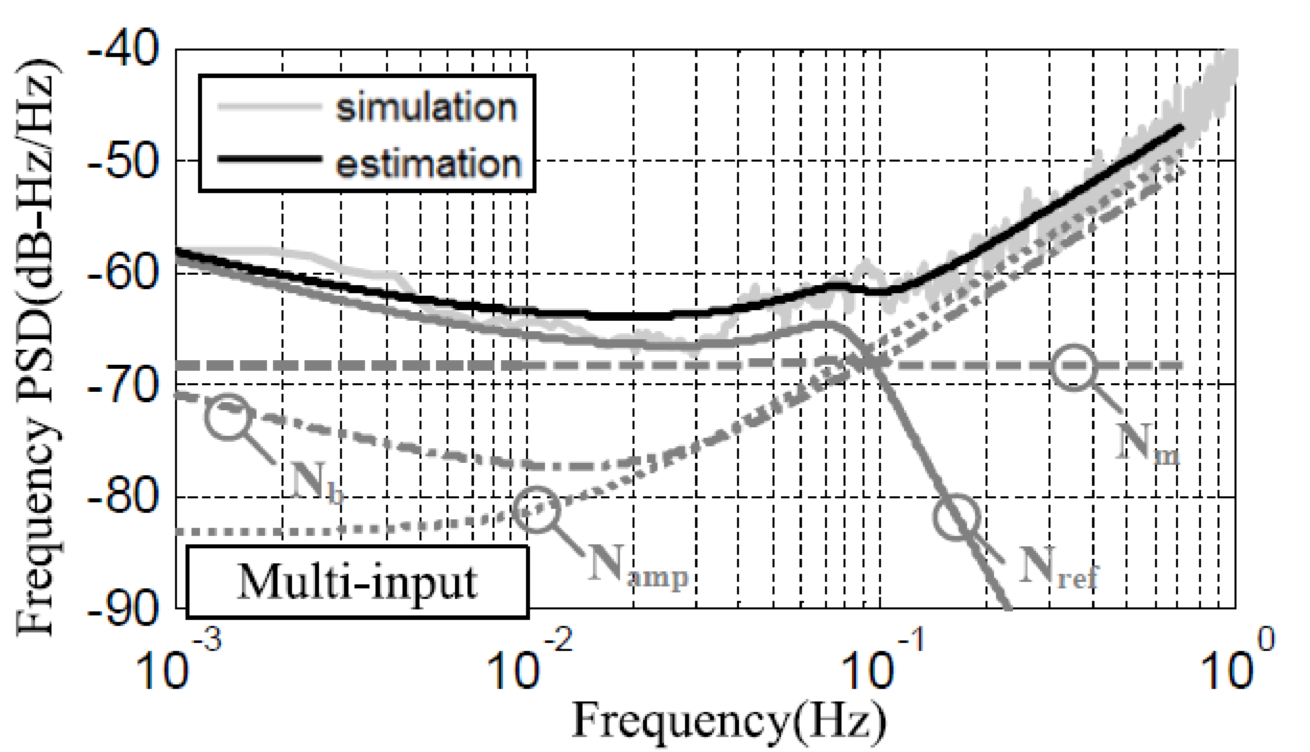
Nonlinearities turned off



Nonlinearities turned on

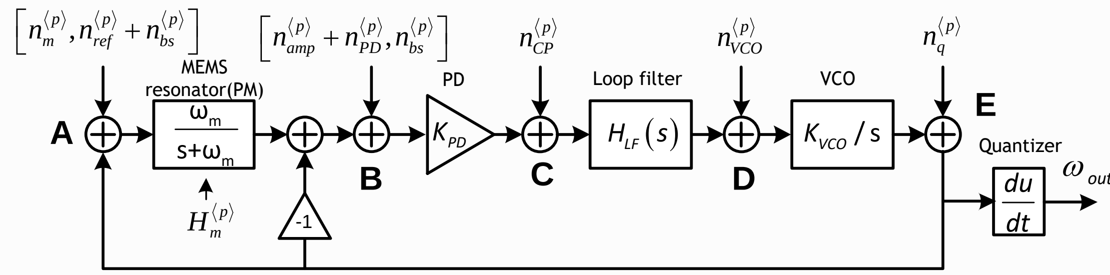
Noise prediction (design guidelines)

- **Noise Contribution Analysis**
  - n_b and n_{ref} contribute 1/f noise
  - n_m contribute only white noise

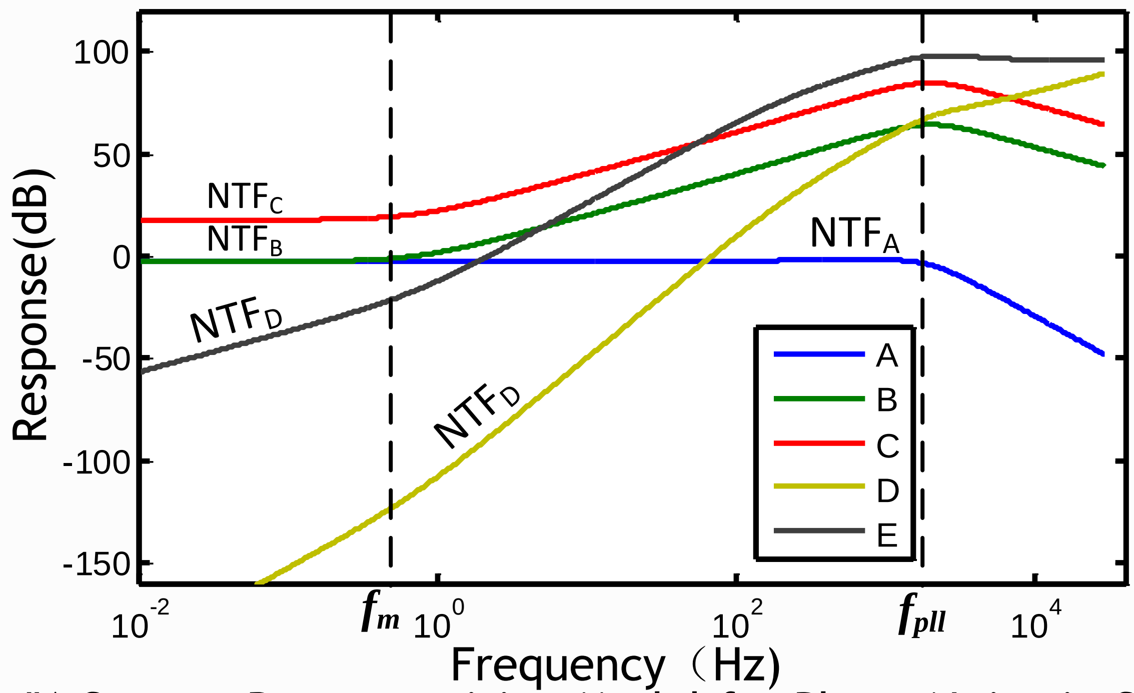


Noise prediction (design guidelines)

System Model:



Noise Prediction:



- Zhao, Jian, et al. "A System Decomposition Model for Phase Noise in Silicon Oscillating Accelerometers." *IEEE Sensors Journal* 16.13 (2016): 5259-5269.

Specification breakdown

- Do not over design! Noise performance and power consumption are trade-off

Specification breakdown

Block name	Flicker noise	White noise
Mixer	1u V/rt Hz @1Hz	100n V/rt Hz
Instrument amplifier	1.3u V/rt Hz @1Hz	161n V/rt Hz
Front-end	---	10f A/rt Hz
Block name	White frequency noise	White phase noise
VCO	-15 dBc @ 1Hz	-60 dBc
Quantizer		-90 dBc

Spec. for Mixer (blk #1)

Spec name	Unit	Specification	Max value	Min value
Input Flicker noise	V/rt Hz@1Hz	600n	2.16 u	
Input White noise	V/rt Hz	100n	70 n	
Gain	uA/V	30	39	22
Input Swing 10% gain loss Under 1.8V		>400mV	725mV	400mV
Input Swing Under 1.5V		>400mV	725mV	400mV
Output Swing		>250 p-p		
Current		<80uA		

Parameter name	Unit	Specification	Max value	Min value
Flicker noise	V/rt Hz@1Hz	1.3u	1.18u	
White noise	V/rt Hz	100n	118n	
Gain		0.8~1	0.86	0.84
output Swing 10% gain loss Under 1.8V	V	[0.9,1,3]	[0.3,1,4]	[0.9,1,3]
Output Swing Under 1.5V	V	[0.9,1,3]	[0.3,1,4]	[0.9,1,3]
Bandwidth	Hz		330kHz	220kHz
Current		<80u	100uA	92uA

Spec. for D2S (blk #2)

Parameter name	Unit	Specification	Max value	Min value
White phase noise	dBc/Hz	<-60	-100	
White frequency noise	dBc/Hz @ 1Hz	-15	-15	
Gain	Hz/V	2M	2.5M	1.6M
Bandwidth				
Current				

Spec. for VCO (blk #4)

Summary

- 1. Flicker noise stem from oscillating amplitude.
- 2. Noise model can provide an accurate prediction, and noise breakdown
- 3. Novel architecture of technique may reduce the flicker noise without additional overheads

Definition & Analysis spend more time than circuit design !!!

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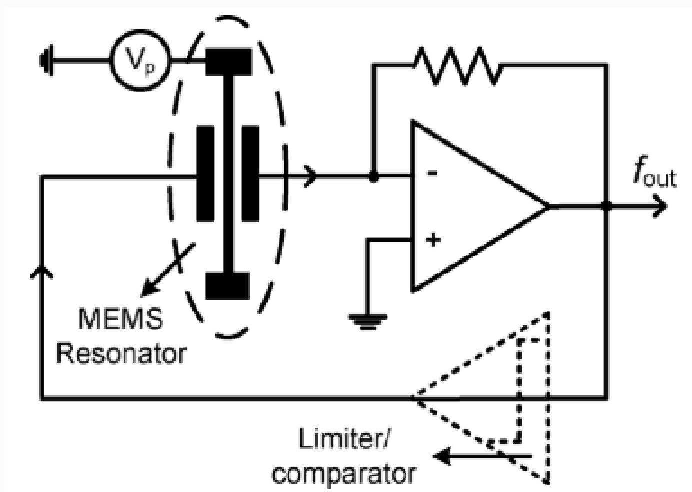
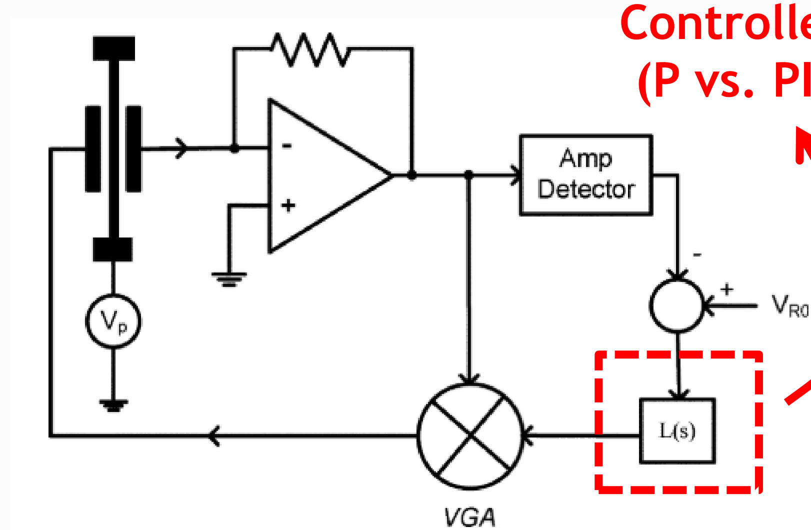
Motivation of the proposed scheme

- Two main measures:
  - Reduce the nonlinearity (amplitude limitation)
  - Attenuate the amplitude flicker noise



Saturation region limits the amplitude
(Non-linear)

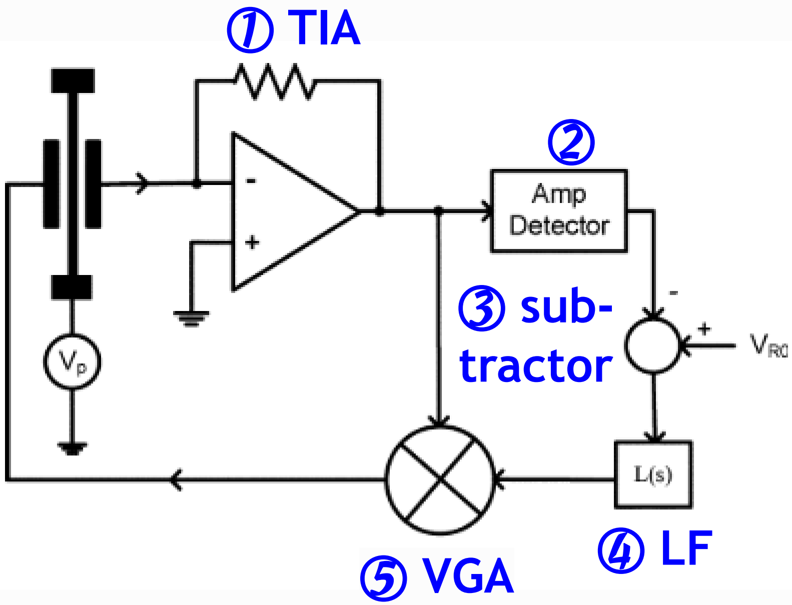
Controller
(P vs. PI)

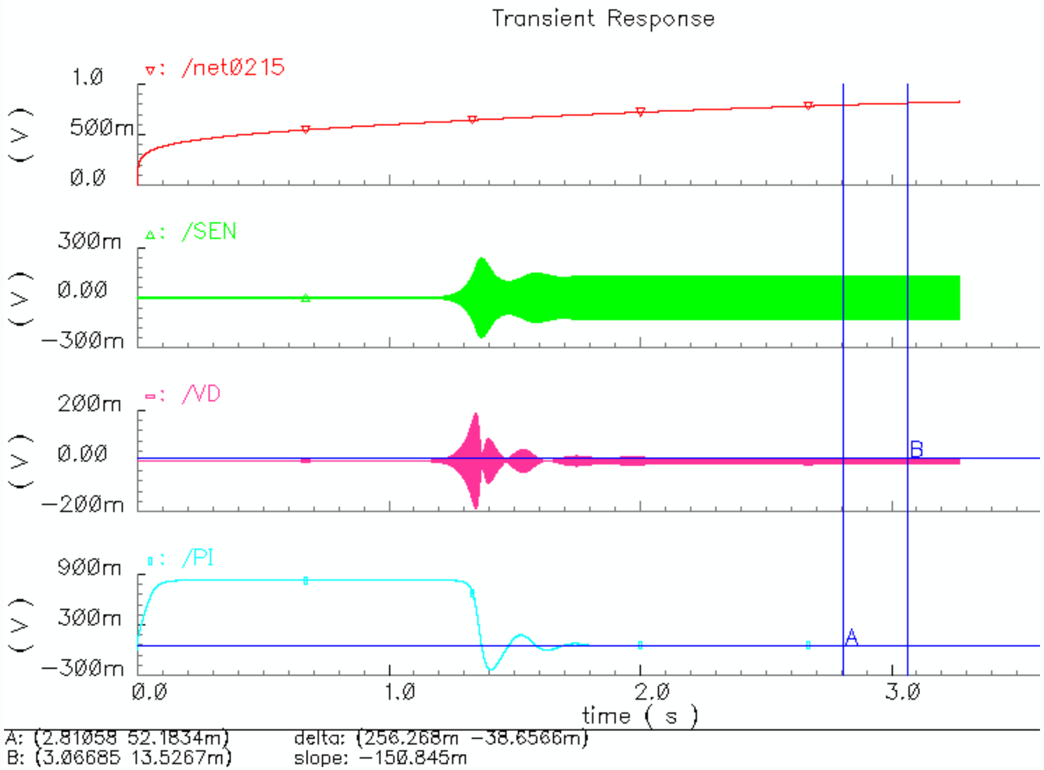


Amplitude control system
(Linear)

Auto amplitude control technique

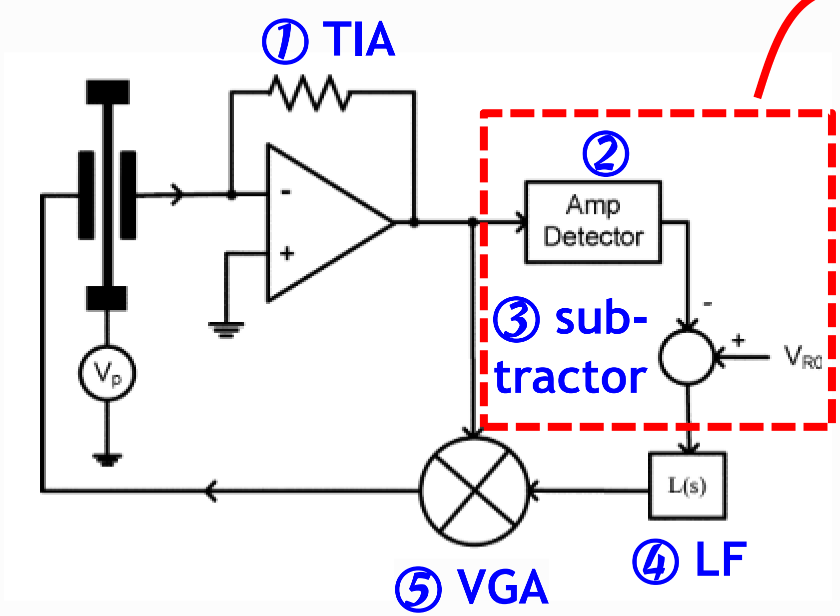
- Functional analysis
- Stability analysis (PVT, monte-carlo)

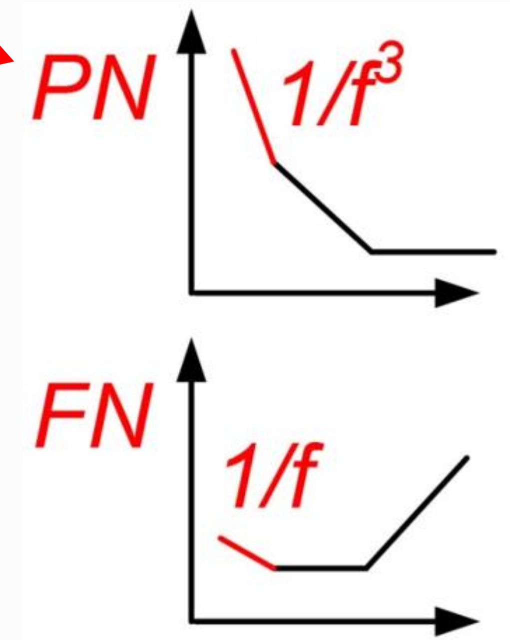




Auto amplitude control technique

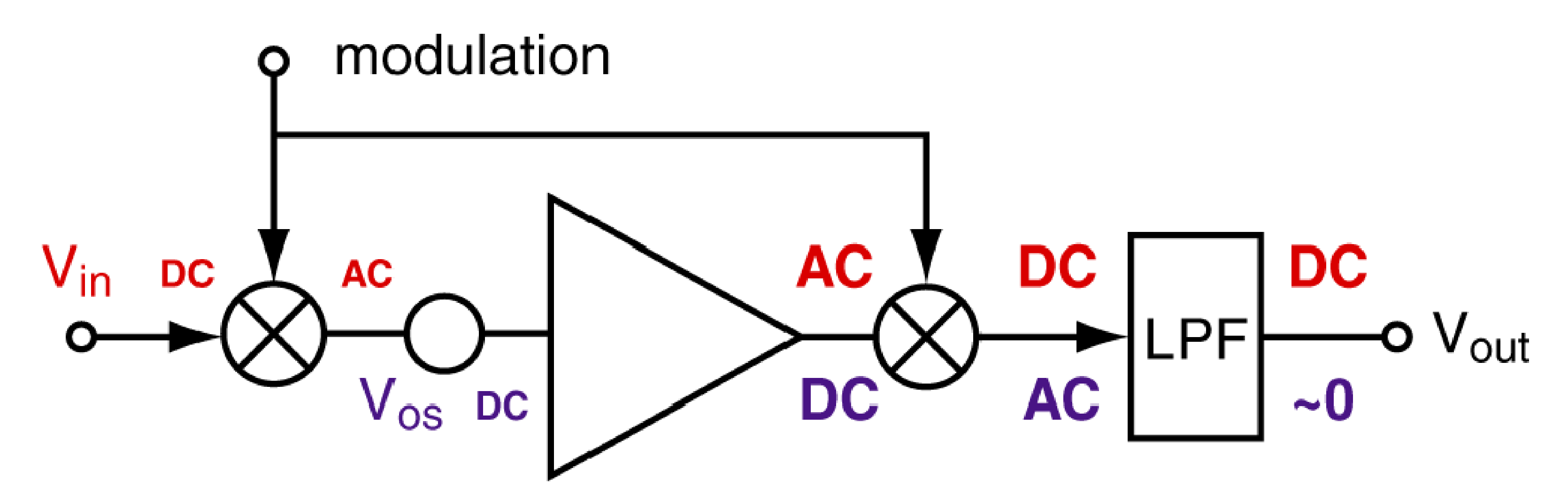
- Noise analysis (using pre-mentioned model)
- Flicker noise stem from the amplitude control circuits

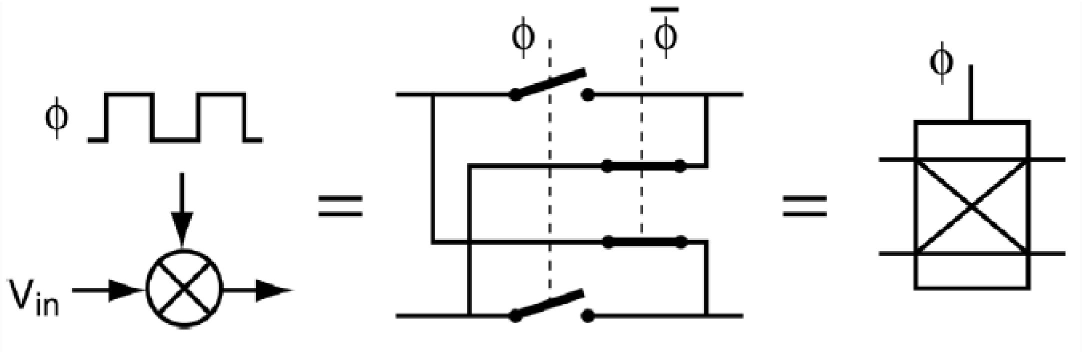




Chopper technique (additive)

- Chopper technique can bypass the flicker noise sources
- Fully differential signals can chop the signal by switch





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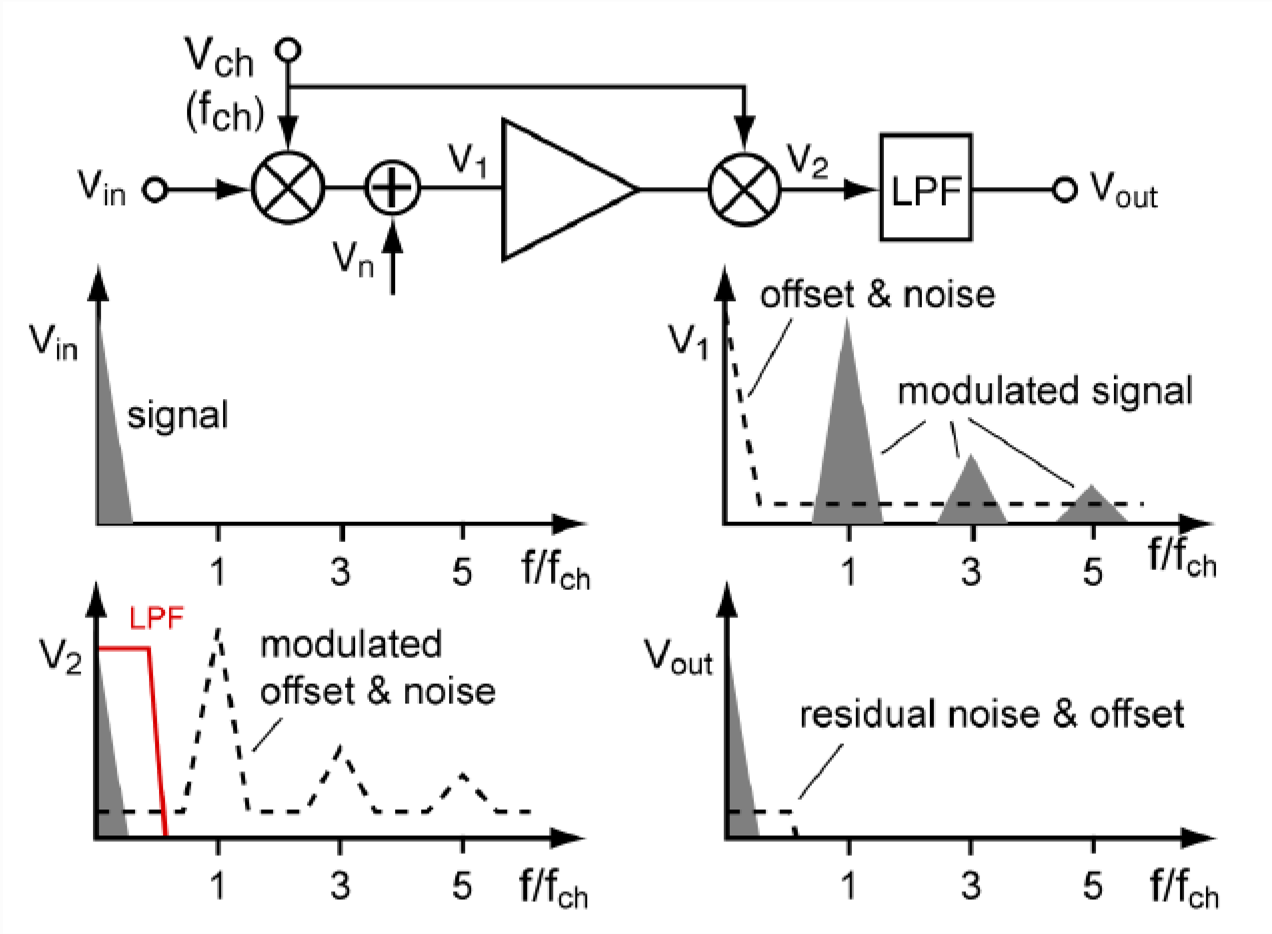

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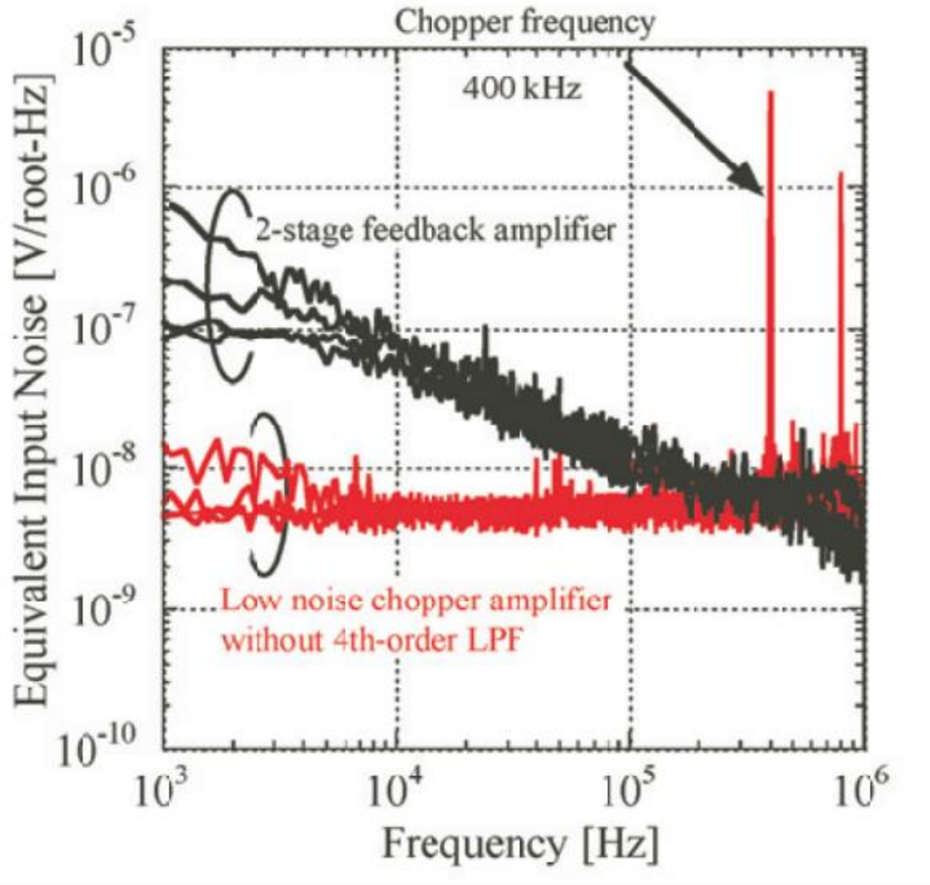
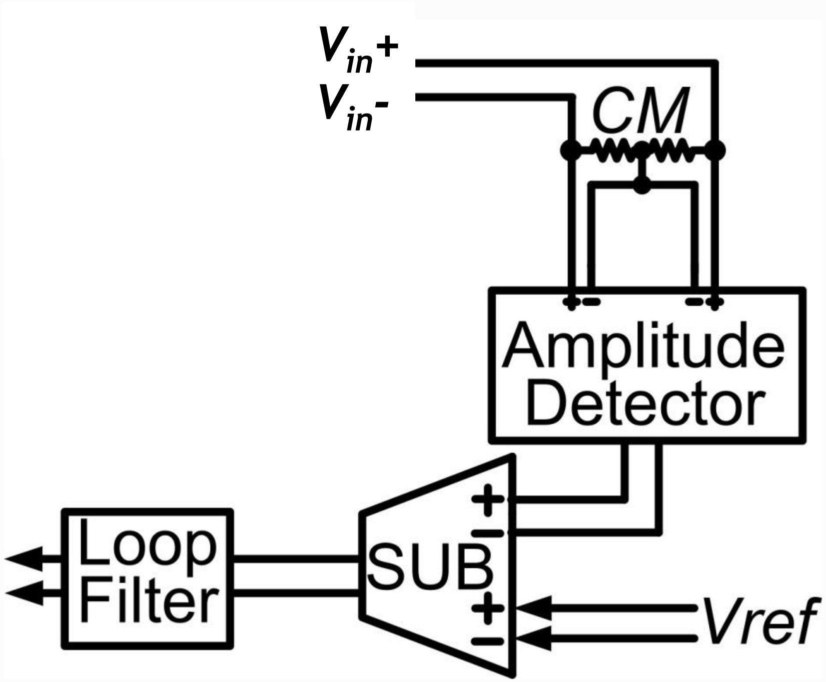
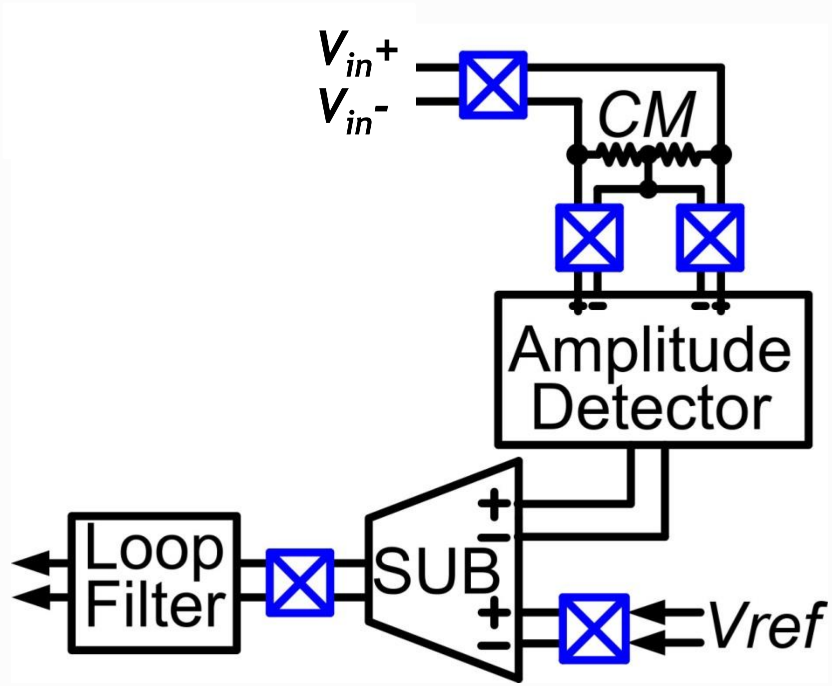


Chopper technique (additive)

- Employing chopper tech. everywhere in DC path



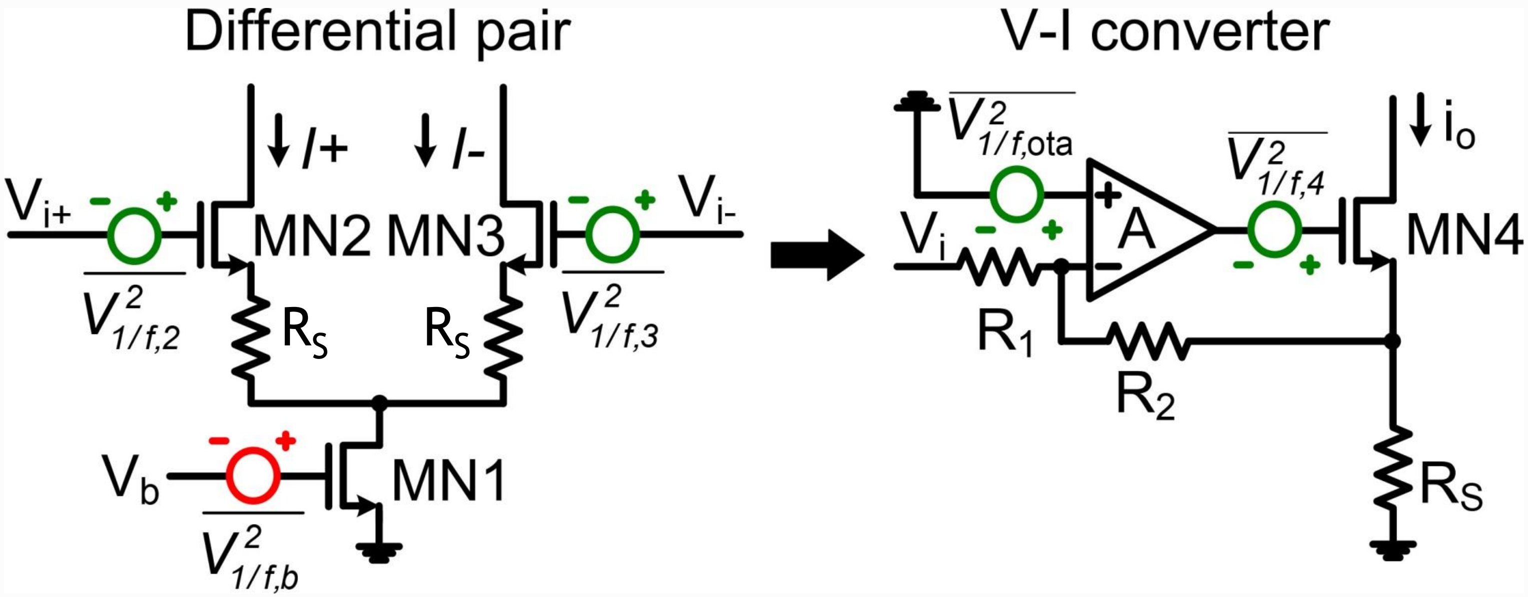
Without Chopper



With Chopper

Gain stability (multiplicative)

- Using negative feedback to stabilize the gain
- Reduce the multiplicative flicker noise

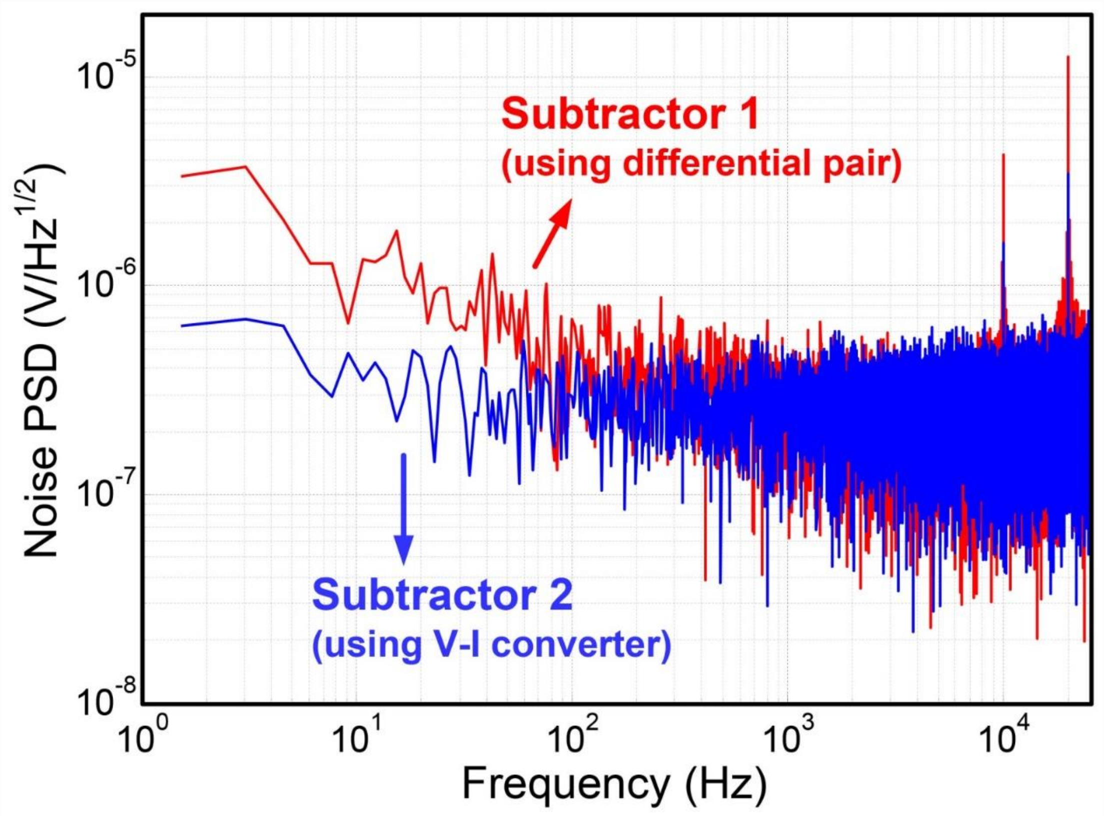


$G_m = g_m / (1 + g_m R_S)$

$G_m = R_1 / (R_S R_2)$

Gain stability (multiplicative)

- Using negative feedback to stabilize the gain
- Reduce the multiplicative flicker noise



Summary

- 1. Auto-amplitude control tech. reduces the nonlinearity.
- 2. Chopper tech. + Boosted Gain V-I converter can reduce the flicker noise source

Outline of Lecture #7

- Motivation
  - Case introduction, design flow
  - Motivation, Previous works review, benchmark
- Specification breakup & Block design
  - Modeling, Specification breakup
- Architecture & Circuit blocks
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- Chip implementation
  - Auxiliary circuit & whole chip layout
- Measurement

Specification breakdown

- Do not over design! Follow the given specification, teamwork is required!

Specification breakdown

Block name	Flicker noise	White noise
Mixer	1u V/rt Hz @1Hz	100n V/rt Hz
Instrument amplifier	1.3u V/rt Hz @1Hz	161n V/rt Hz
Front-end	---	10f A/rt Hz
Block name	White frequency noise	White phase noise
VCO	-15 dBc @ 1Hz	-60 dBc
Quantizer		-90 dBc

Spec. for Mixer (blk #1)

Spec name	Unit	Specification	Max value	Min value
Input Flicker noise	V/rt Hz@1Hz	600n	2.16 u	
Input White noise	V/rt Hz	100n	70 n	
Gain	uA/V	30	39	22
Input Swing 10% gain loss Under 1.8V		>400mV	725mV	400mV
Input Swing Under 1.5V		>400mV	725mV	400mV
Output Swing		>250 p-p		
Current		<80uA		

Parameter name	Unit	Specification	Max value	Min value
Flicker noise	V/rt Hz@1Hz	1.3u	1.18u	
White noise	V/rt Hz	100n	118n	
Gain		0.8~1	0.86	0.84
output Swing 10% gain loss Under 1.8V	V	[0.9,1,3]	[0.3,1,4]	[0.9,1,3]
Output Swing Under 1.5V	V	[0.9,1,3]	[0.3,1,4]	[0.9,1,3]
Bandwidth	Hz		330kHz	220kHz
Current		<80u	100uA	92uA

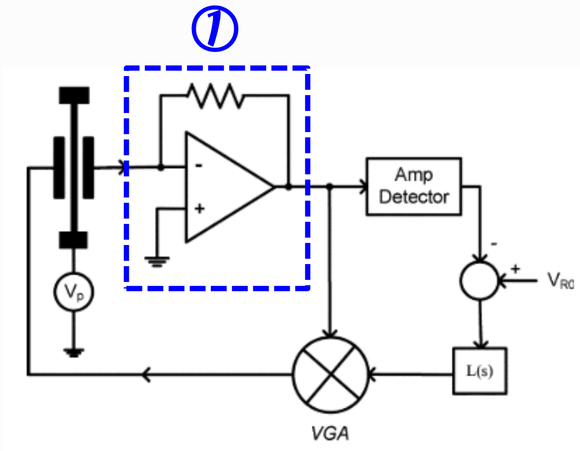
Spec. for D2S (blk #2)

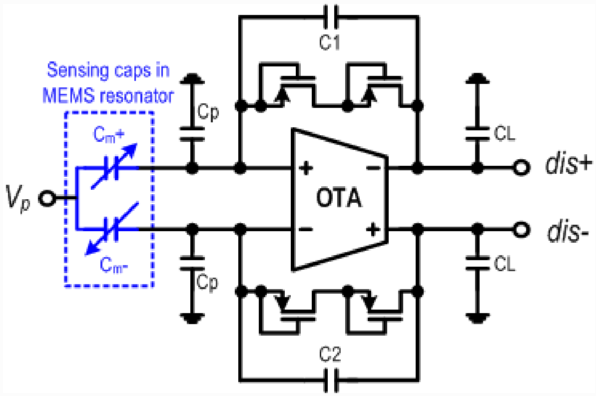
Parameter name	Unit	Specification	Max value	Min value
White phase noise	dBc/Hz	<-60	-100	
White frequency noise	dBc/Hz @ 1Hz	-15	-15	
Gain	Hz/V	2M	2.5M	1.6M
Bandwidth				
Current				

Spec. for VCO (blk #4)

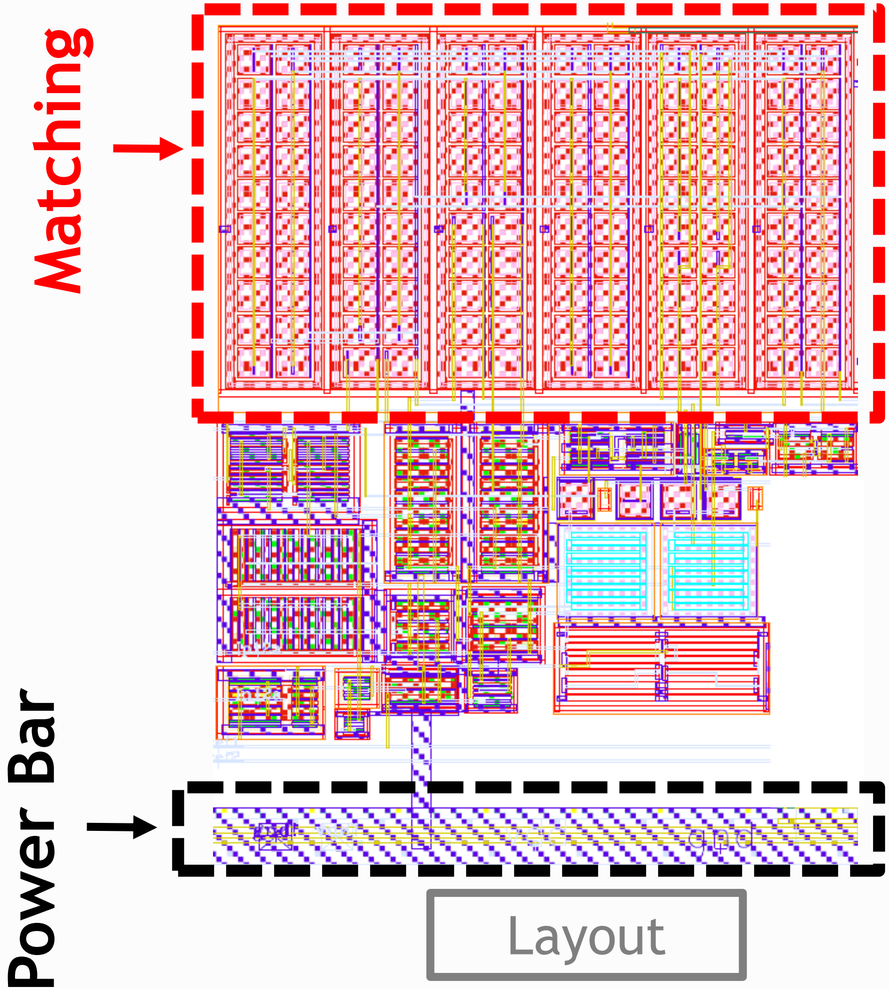
Front-end amplifier

- Pay attention to the capacitive array





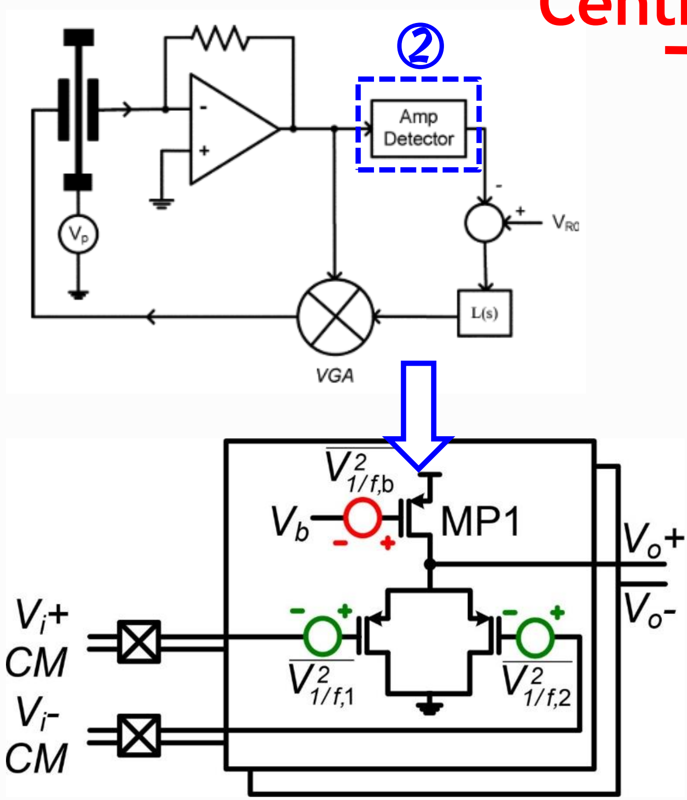
Schematic



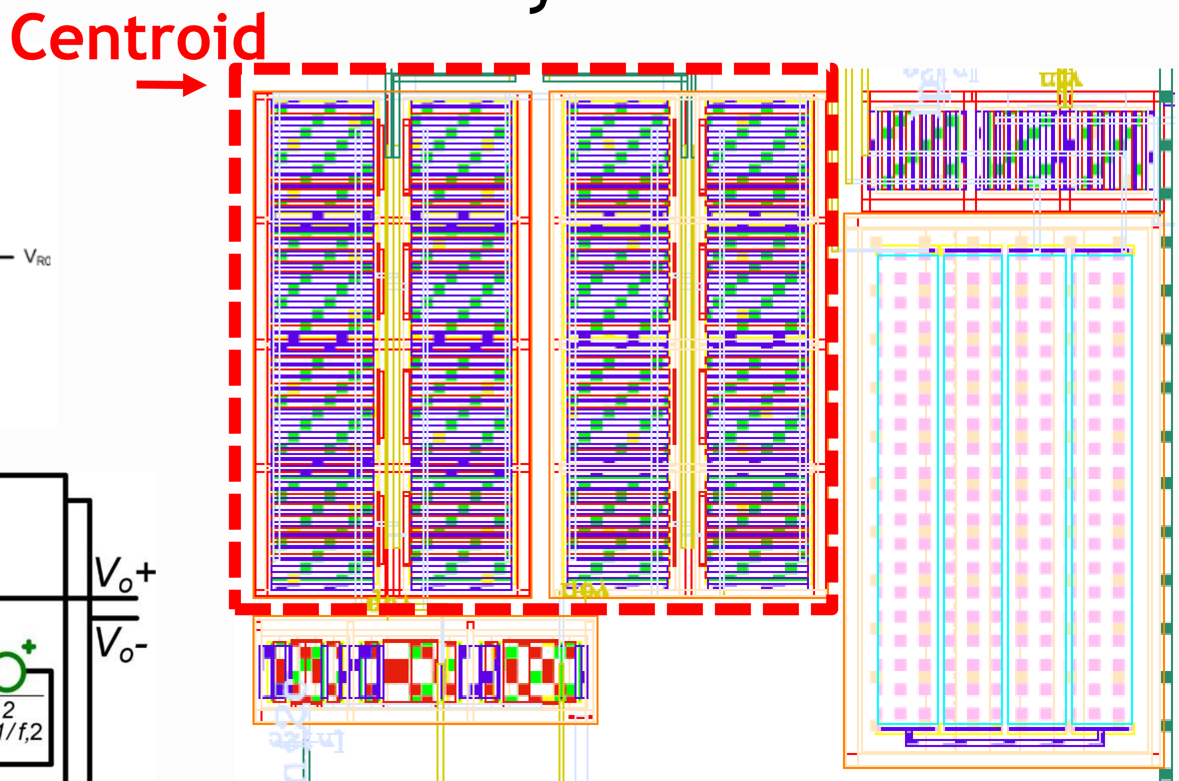
Layout

Amplitude detector

- Amplitude detector has symmetric I/O resp.
- Utilize the 2nd order nonlinearity



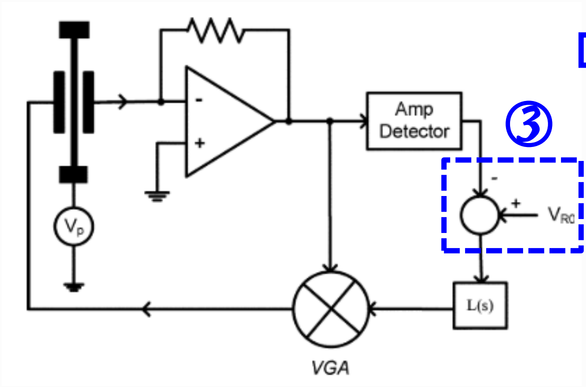
Schematic

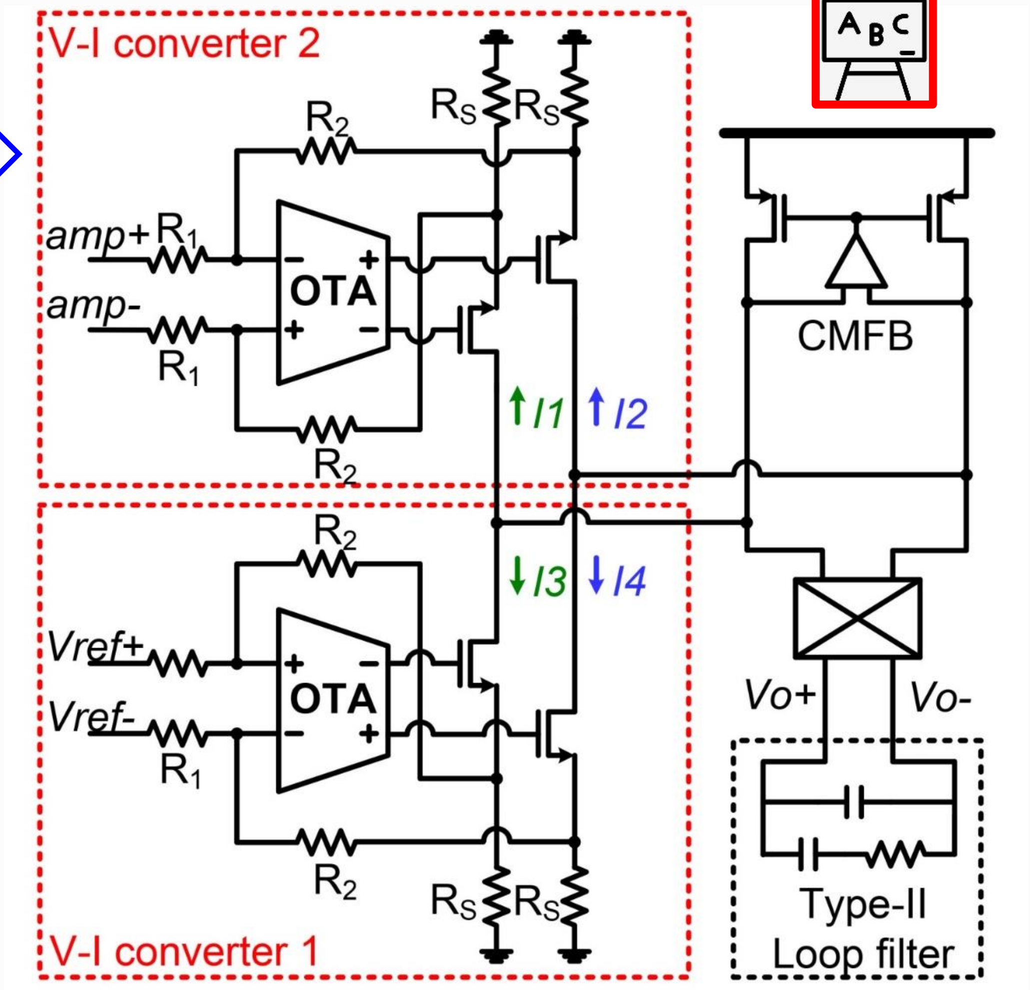


Layout

Subtractor

- Join the outputs of two gm blocks to achieve subtraction





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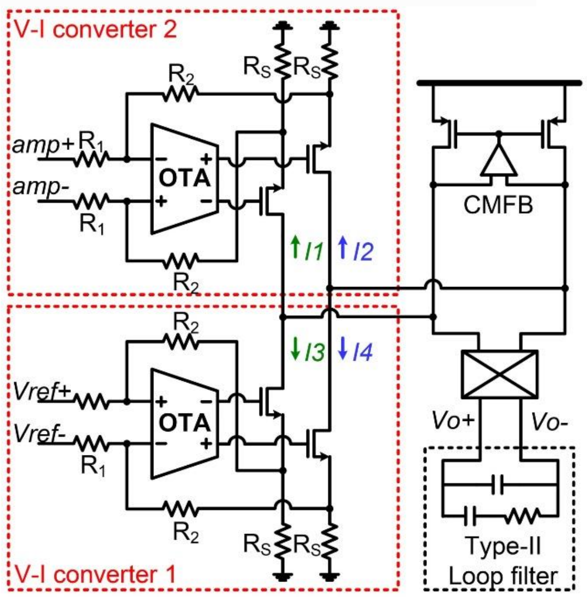
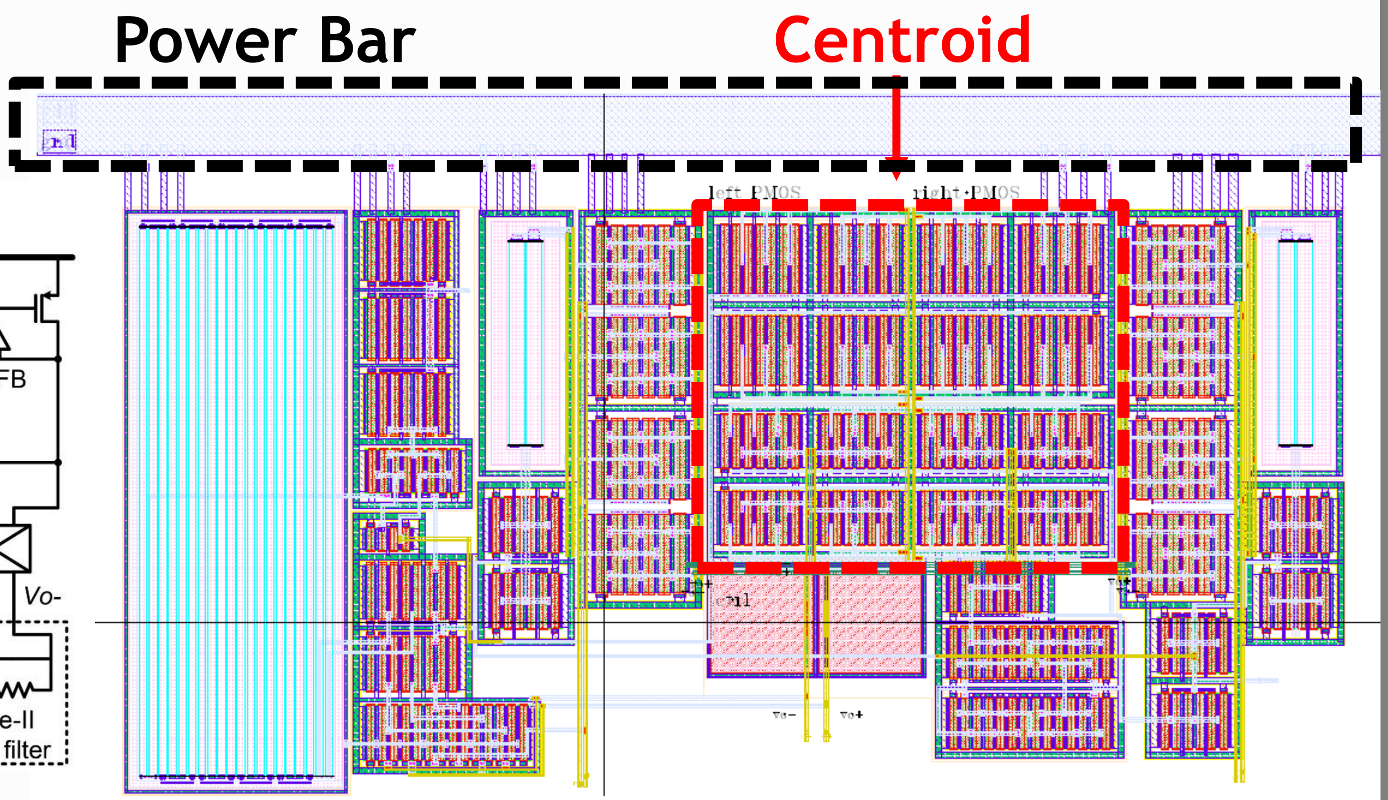


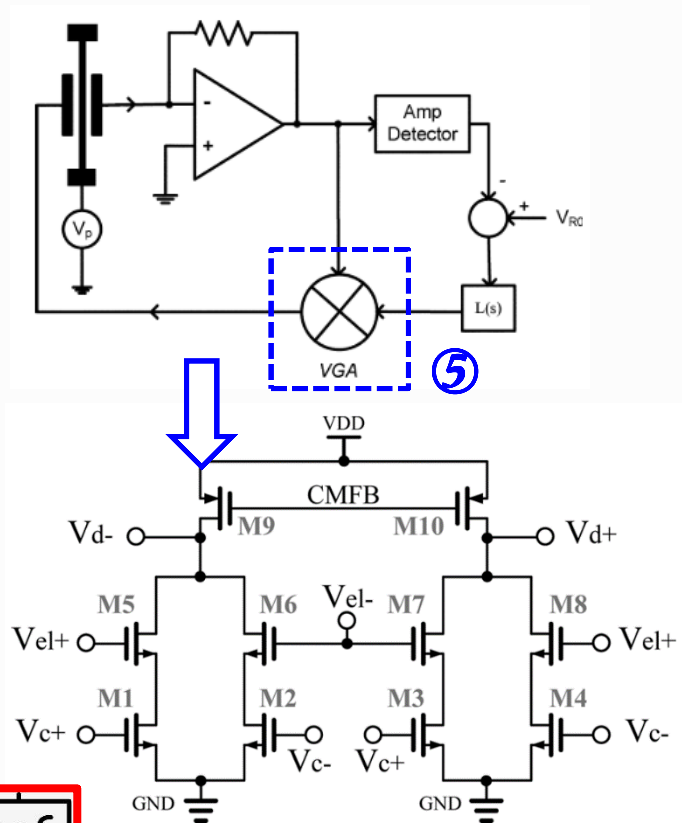
Schematic



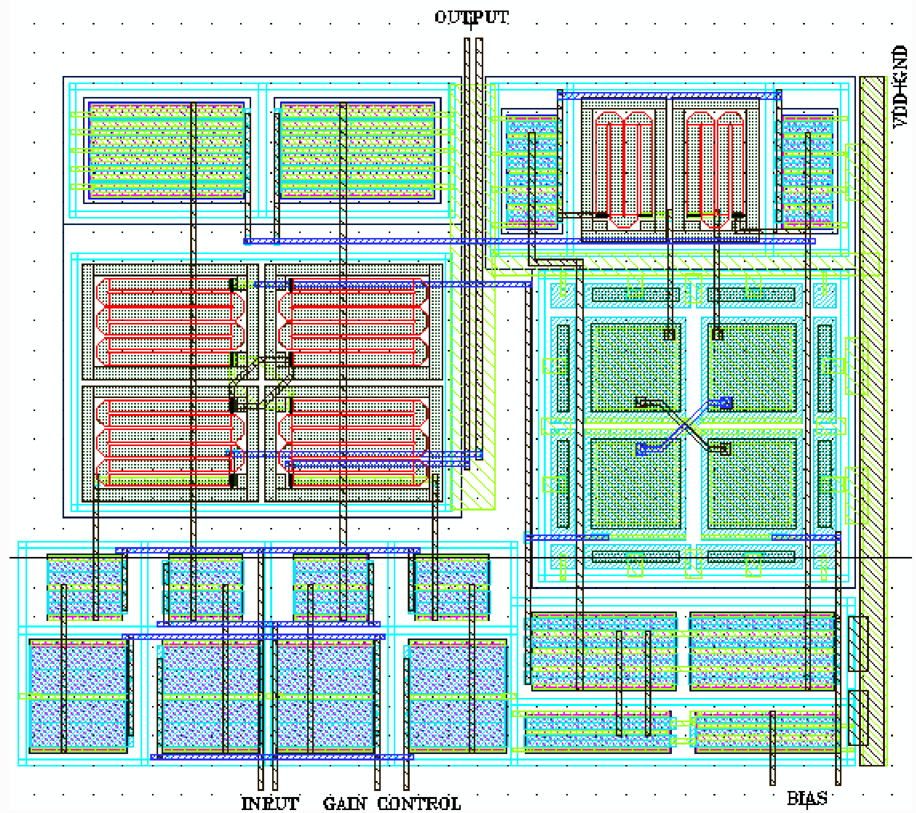
Layout

Multiplier

- High linearity & I/O swing VGA
- Bottom FETs are operating in linear region



Schematic



Layout

Summary

- 1. Chopper technique can lower the flicker noise without additional overhead
- 2. Be careful to the multiplicative flicker noise
- 3. Novel architecture may provide a better solution

Innovations in 3 aspects:
1. Principle level, 2. Architecture level,
3.Circuit level

Utilize the trade-off,
Go beyond the trade-off !!! (innovation)

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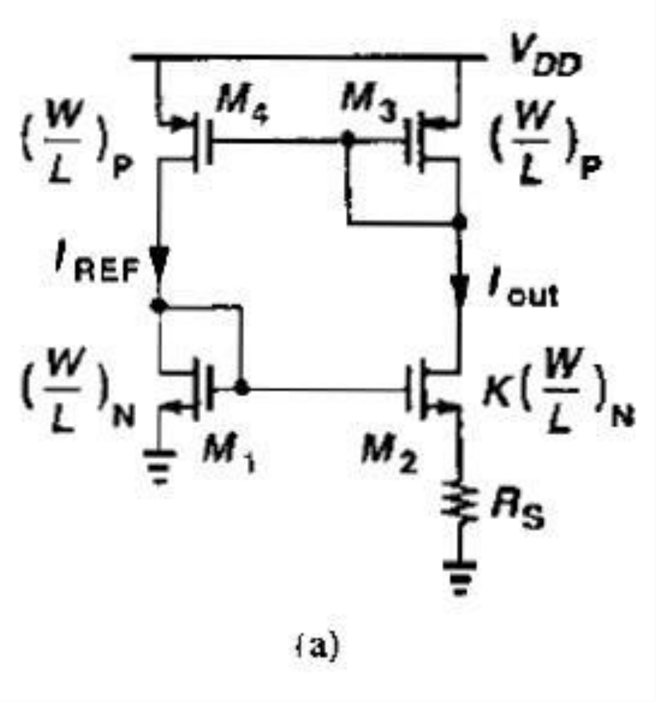
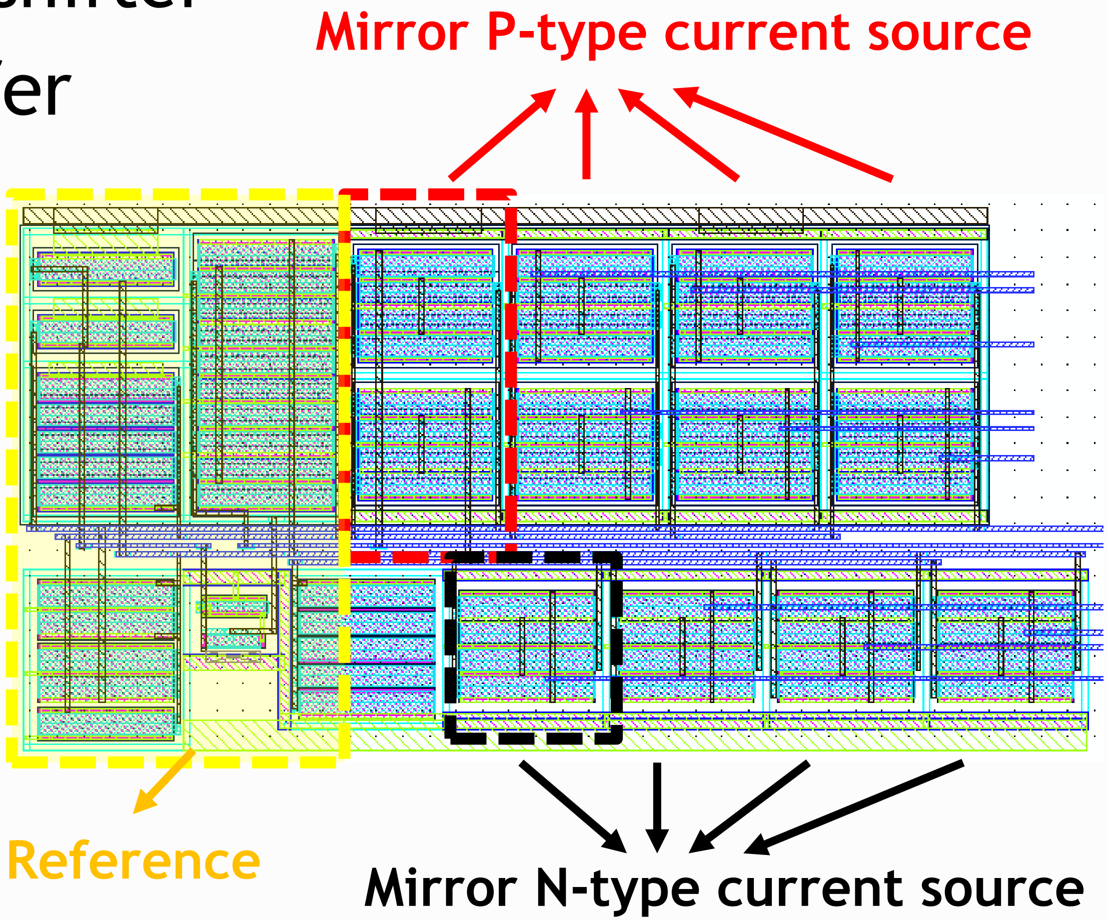
Auxiliary Circuit Blocks

- 1. Current source
- 2. Digital & level shifter
- 3. Analog I/O buffer





Auxiliary Circuit Blocks

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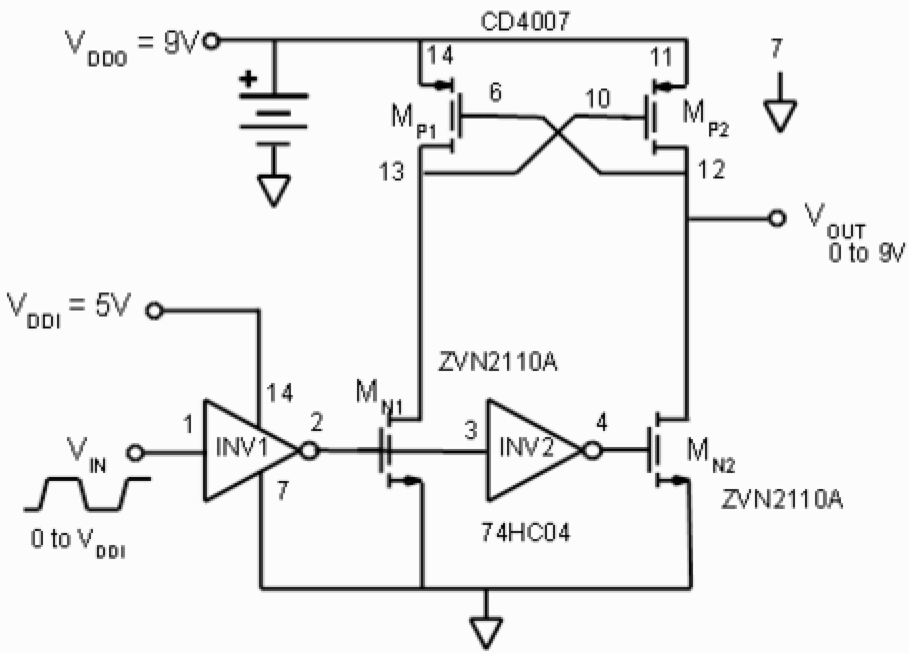
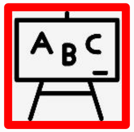
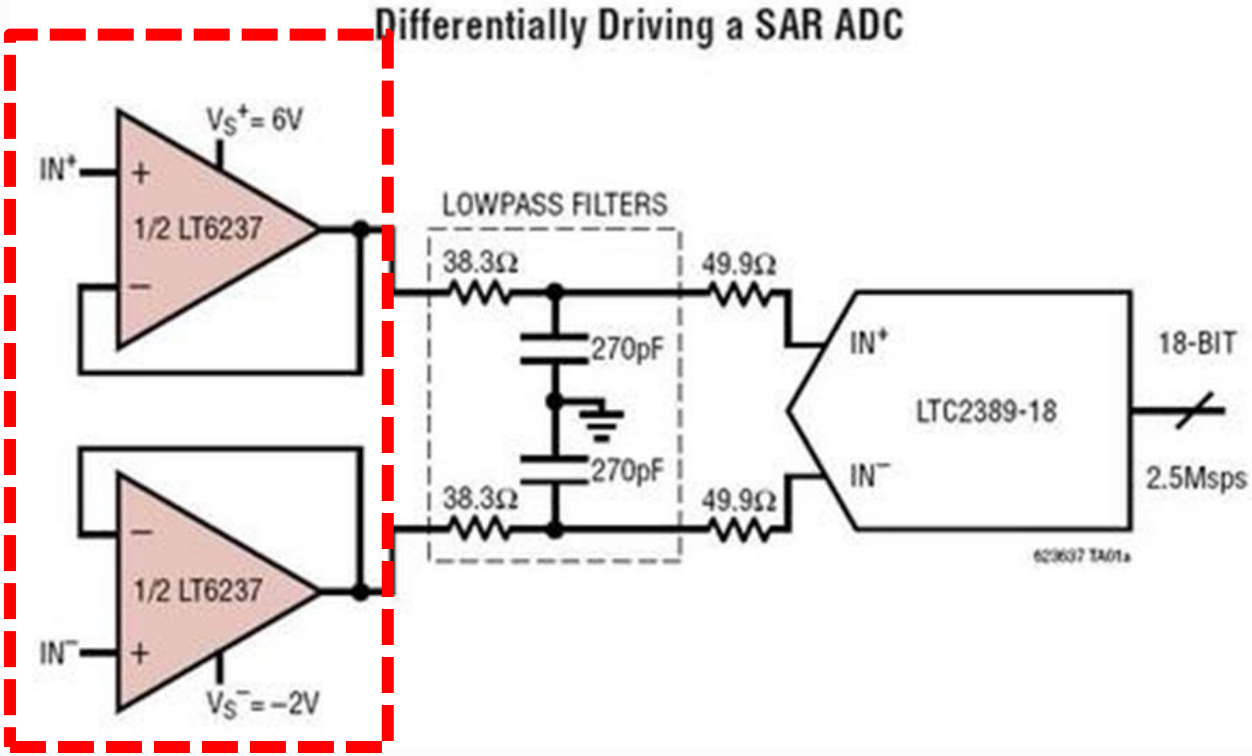


Auxiliary Circuit Blocks

- 1. Current source
- 2. Digital & level shifter
- 3. Analog I/O buffer (place near the previous stage)

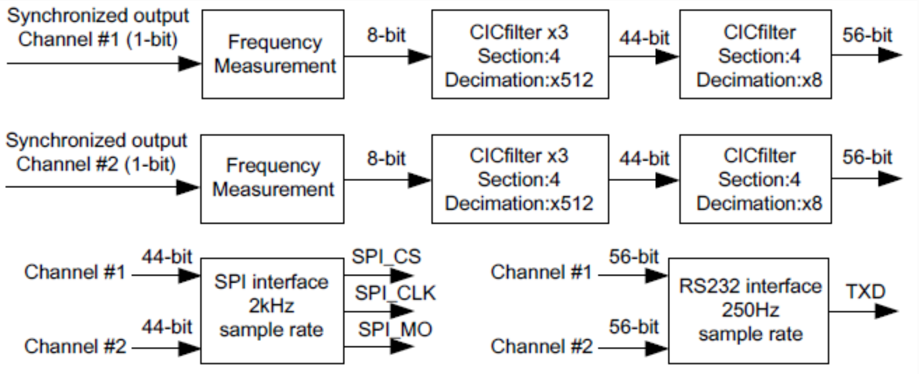


High bandwidth Follower

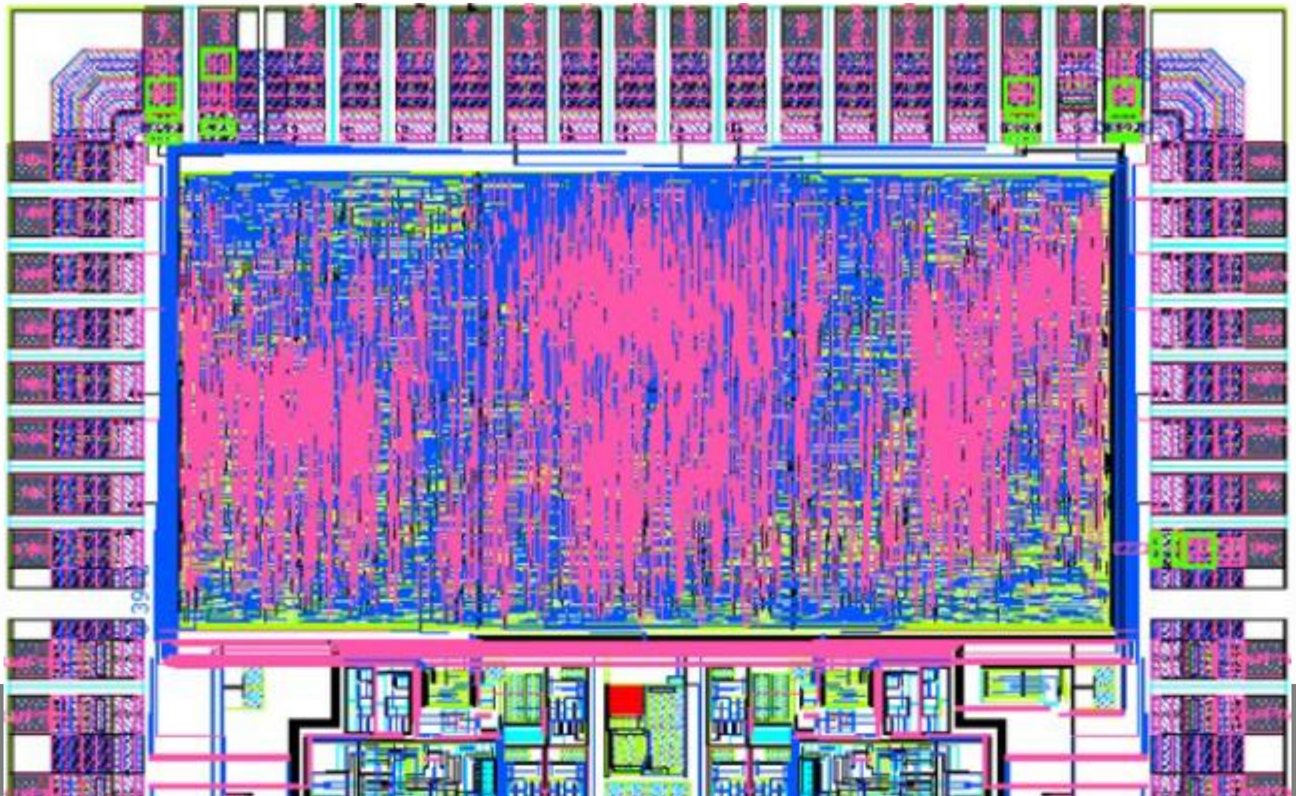


Auxiliary Circuit Blocks

- 1. Current source
- 2. Digital & level shifter
- 3. Analog I/O buffer
- 4. Digital



Estimate the area first!!!
Especially for old process.
(0.18, 0.35)



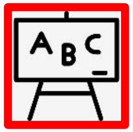
PAD frame

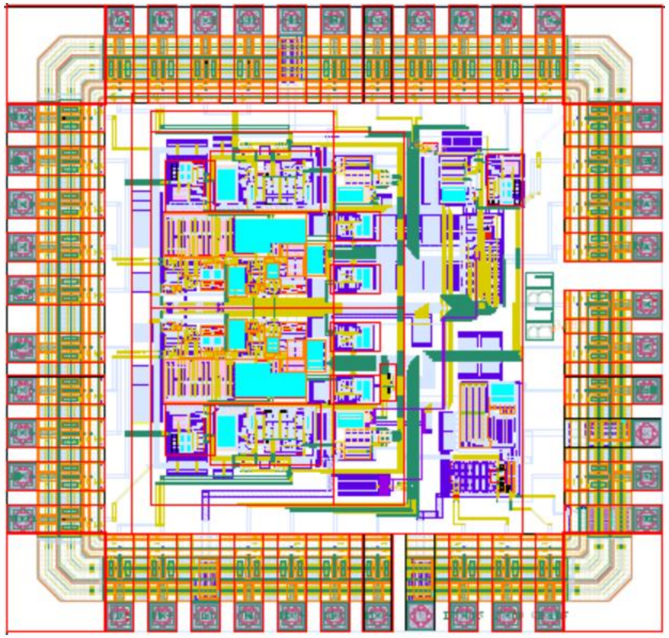
- Refer to PDF file. [mems_acc2]
- 1. PAD frame has two power domain
- 2. Appropriate arrange the wire
  - Follow PAD driven, Block driven, Signal driven rules
- 3. Use decoupling/dummy

  To fill the space

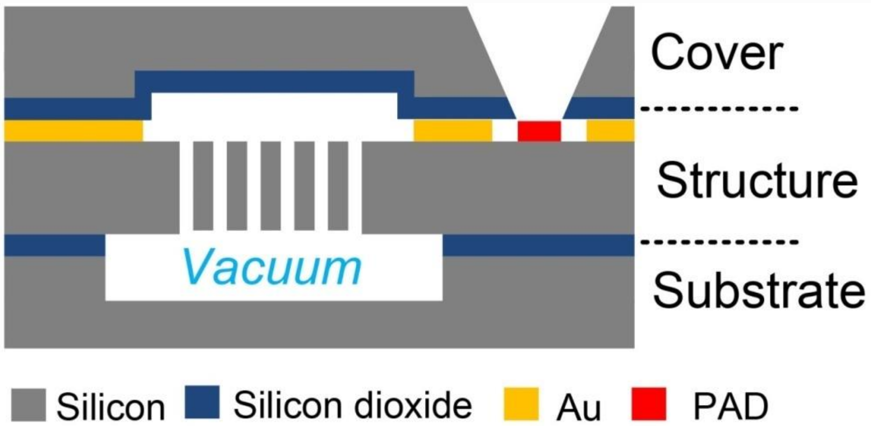
  (density rules,

  ripples in power supply)

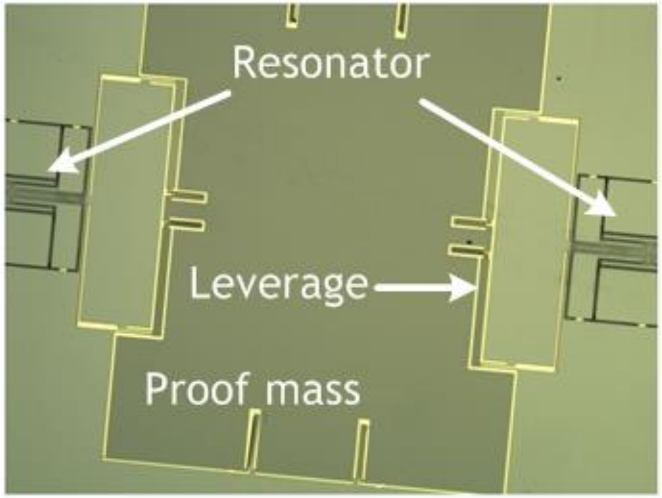




MEMS Sensor

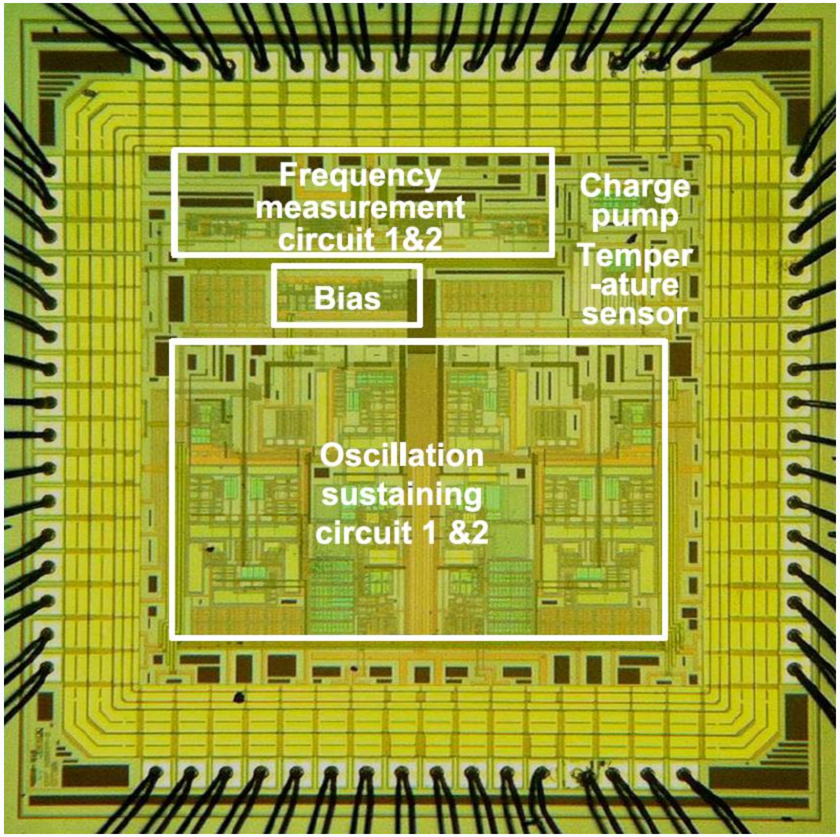


Design performances	
Nominal frequency	20kHz
Quality factor	15000
Scale factor	200Hz/g
Full scale	±30g



Structure layer thickness	SOI 80μm
Comb gap	3μm
Comb overlap length	3μm
Resonant beam length	1mm
Resonant beam width	8μm
Proof mass area	8.43mm^2

Chip Die-photos



- Process: ROIC (CMOS 0.35μm), MEMS (SOI 80μm thickness)
- Area: ROIC ($10mm^2$), MEMS ($20mm^2$)

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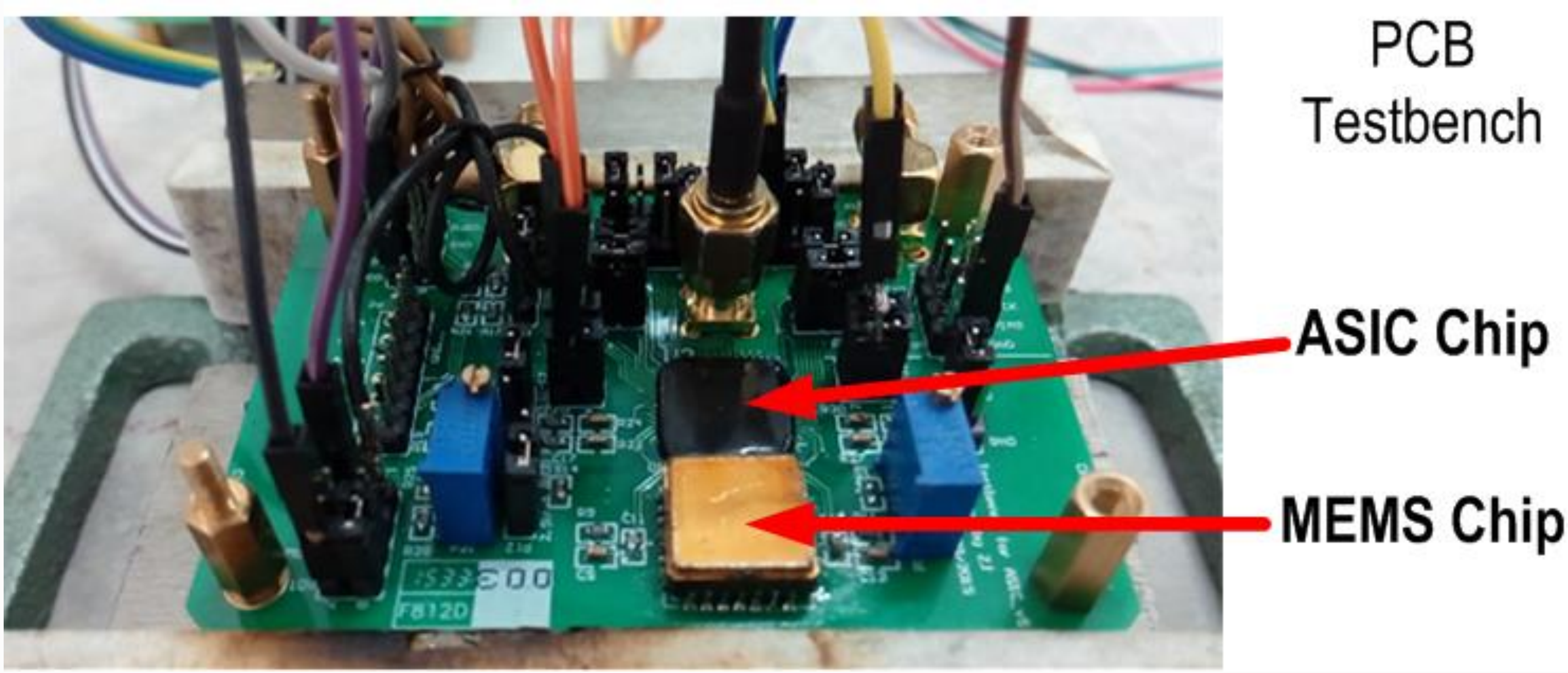
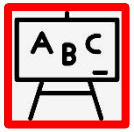
Test bench



- Clock Frequency: 750kHz
- Power Consumption: 2.7mW

Tips during CHIP testing

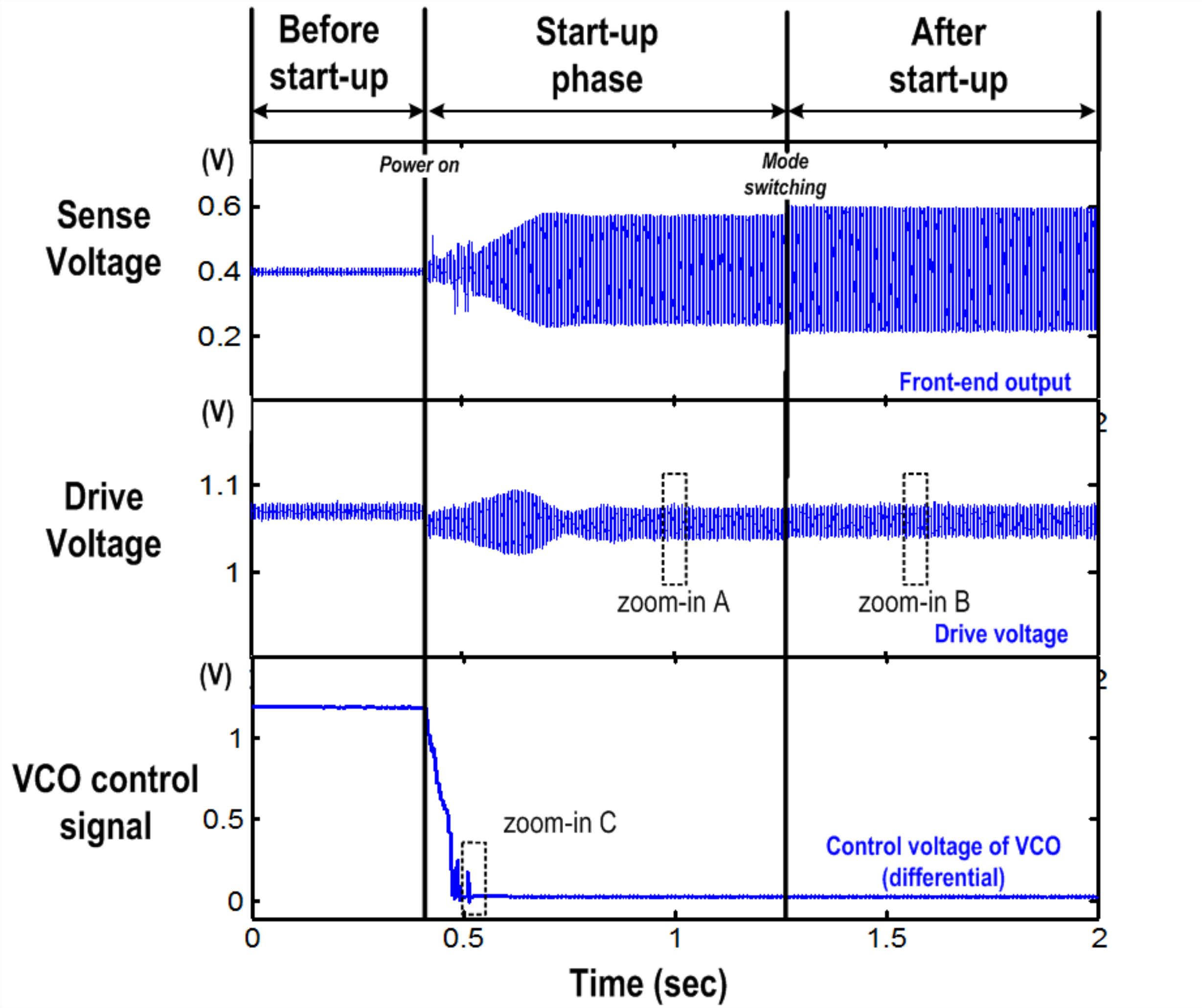
- 1. Use buffer and active probe correctly
- 2. Good performance cannot be achieved without carefully test.



Typical characteristics

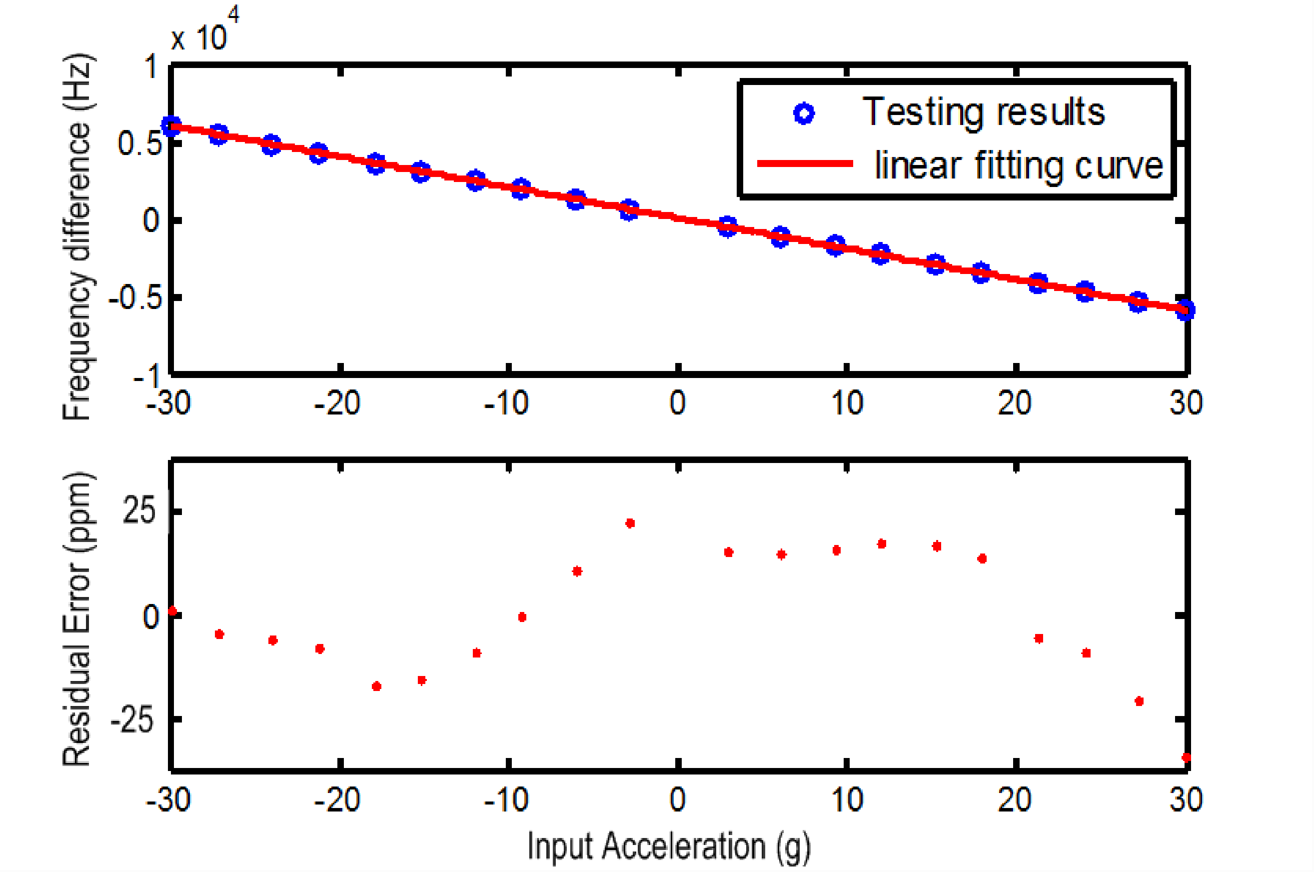
Bandwidth	4.0 GHz
DC resistance	20 kΩ
Input capacitance	<1 pF
Dynamic range	±2 V
Offset range	±5 V

Start-up Measurement



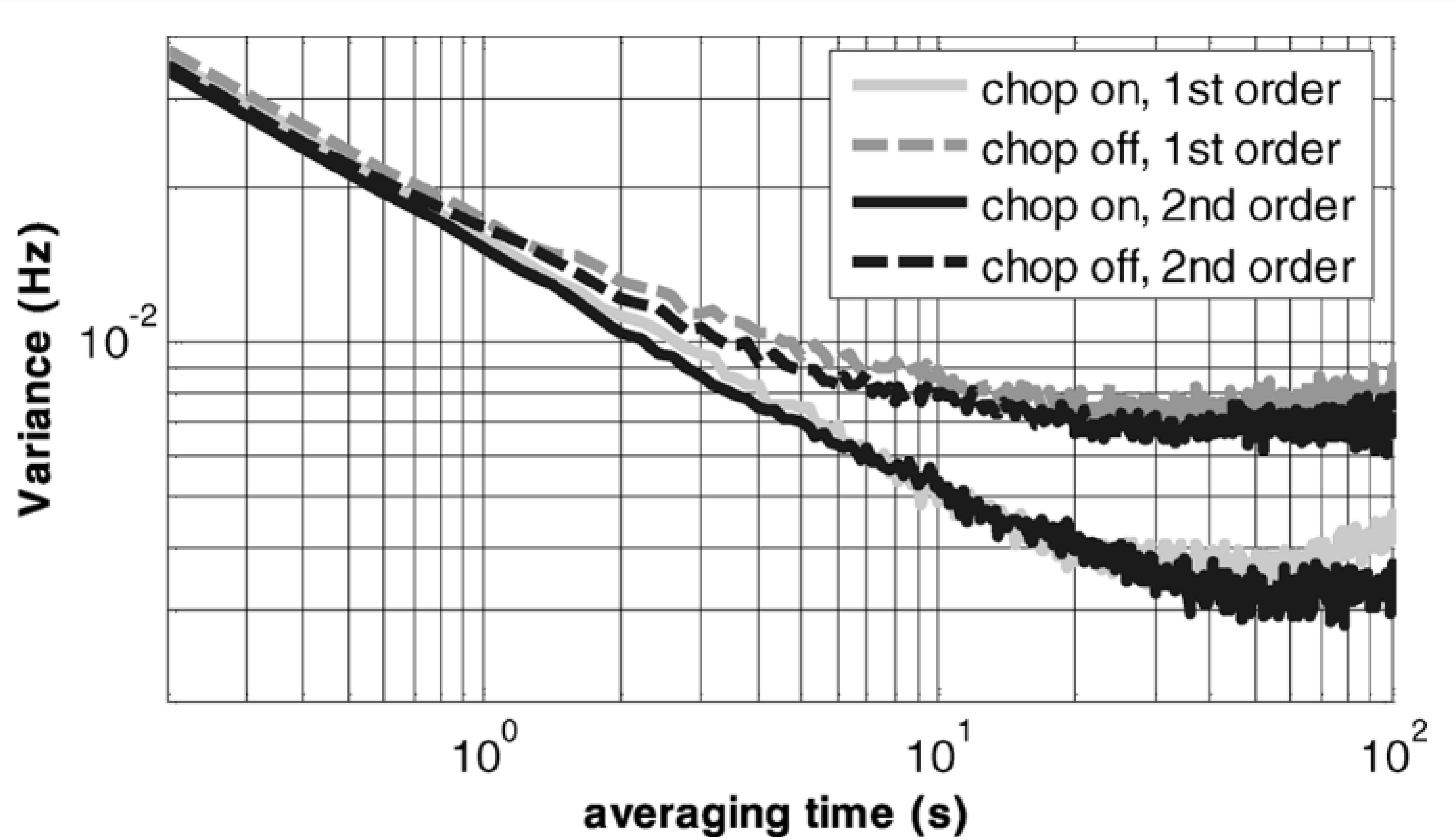
- Recorded by NI-6366 DAQ under 100kHz sample rate

Centrifugal Testing

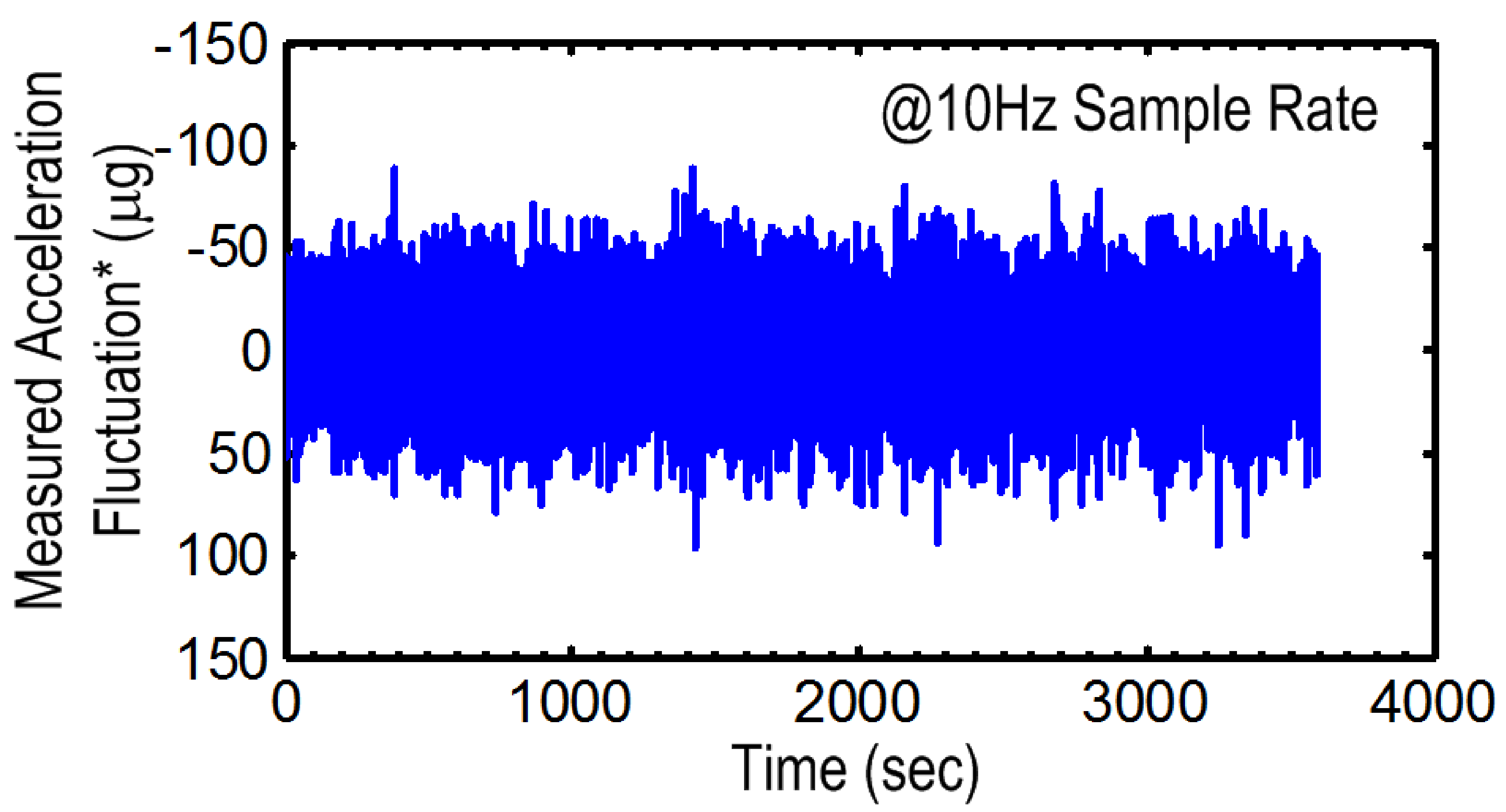


- Full-scale: ±30g   Scale-factor: 190Hz/g
- Nonlinearity: 50ppm

Chopper testing

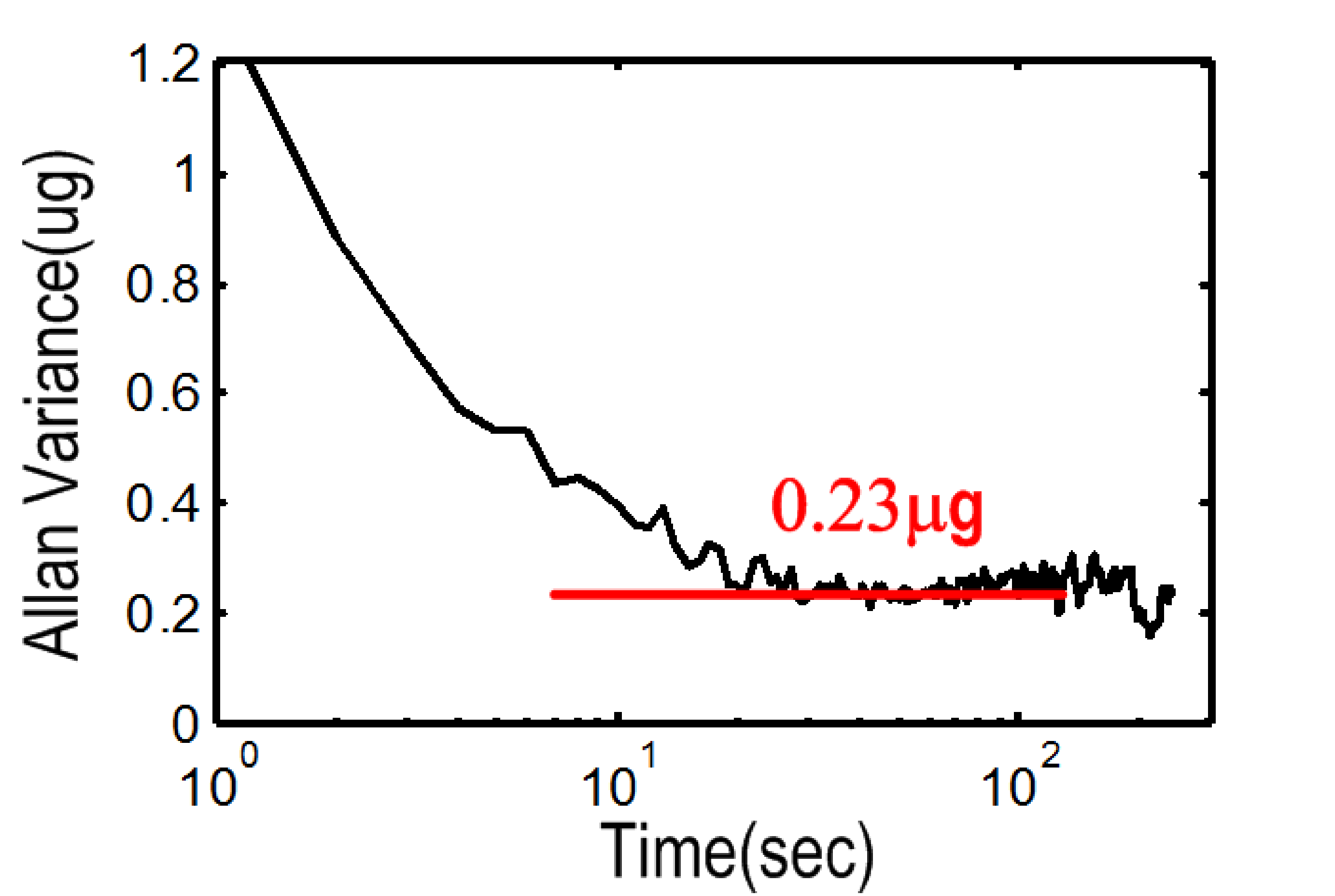


Zero-Input Static Testing



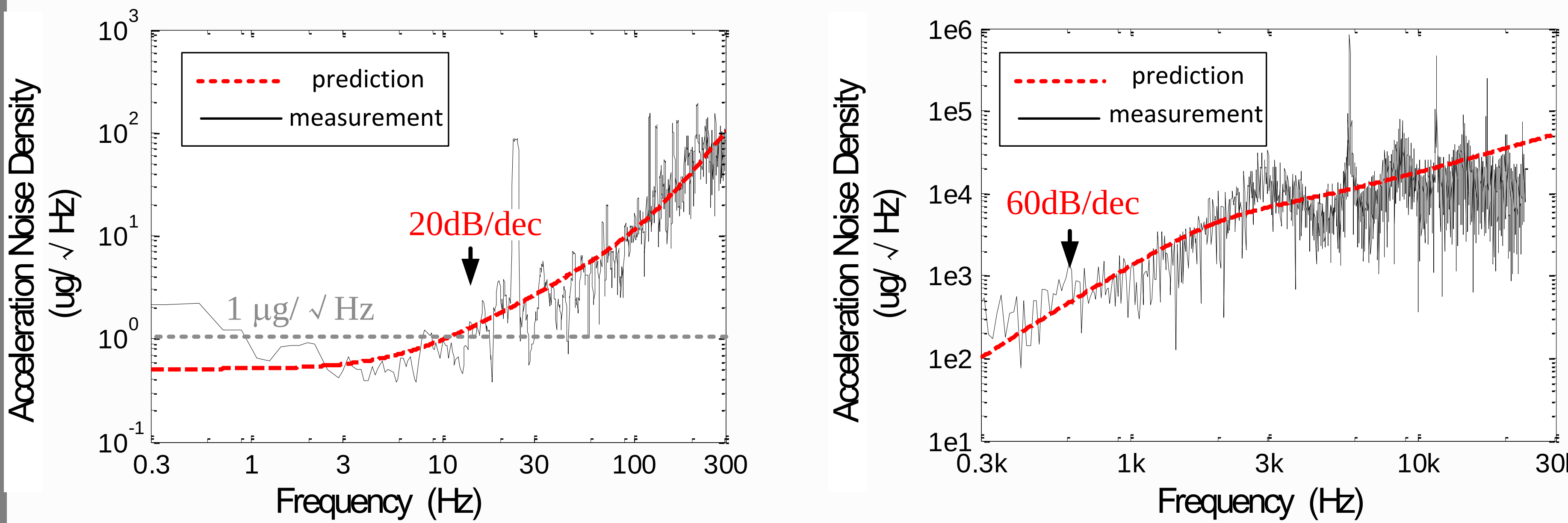
- Bias stability – 1σ (10Hz BW): 17μg
- Bias stability – 1σ (1Hz BW): 2.5μg

Allan Variance



- Bias instability (Allan variance floor): 0.23 μg @30s

Output Power Spectrum Density



（a） LF region　　（b） HF region

- white noise level: 1 μg/√Hz (@frequency < 20Hz)
- Model prediction meet well with the measurement result

Performance Comparison

Parameter	ISSCC'15	JMM'15	ISS'15	JSSC'15	JSSC'12	This work
Mechanism	SOA	SOA	Capacitive	Capacitive	Capacitive	SOA
Process(μm)	0.35	0.35	NA	0.5	0.35	0.35
Supply (V)	1.5	3.3	NA	7	3.6	1.5
Full scale (g)	±20	±20	±15	±1.2	±1.15	±30
Power (mW)	4.4	23	400	23	3.6	2.7
Bias instability (μg)	0.4	4	0.8	18	13	0.23
Noise density (μg/√Hz)	1.2	20	1	0.2	2	1
Relative Instability* (ppb)	10	100	27	7500	5650	4
Relative noise density** (ppb/√Hz)	30	500	33	83	870	17
Readout	AAC based oscillator	AAC based oscillator	Σ–Δ ADC	Σ–Δ ADC	Σ–Δ ADC	PLL based oscillator

* Relative instability = bias instability / full scale

**Relative noise density= noise density / full scale

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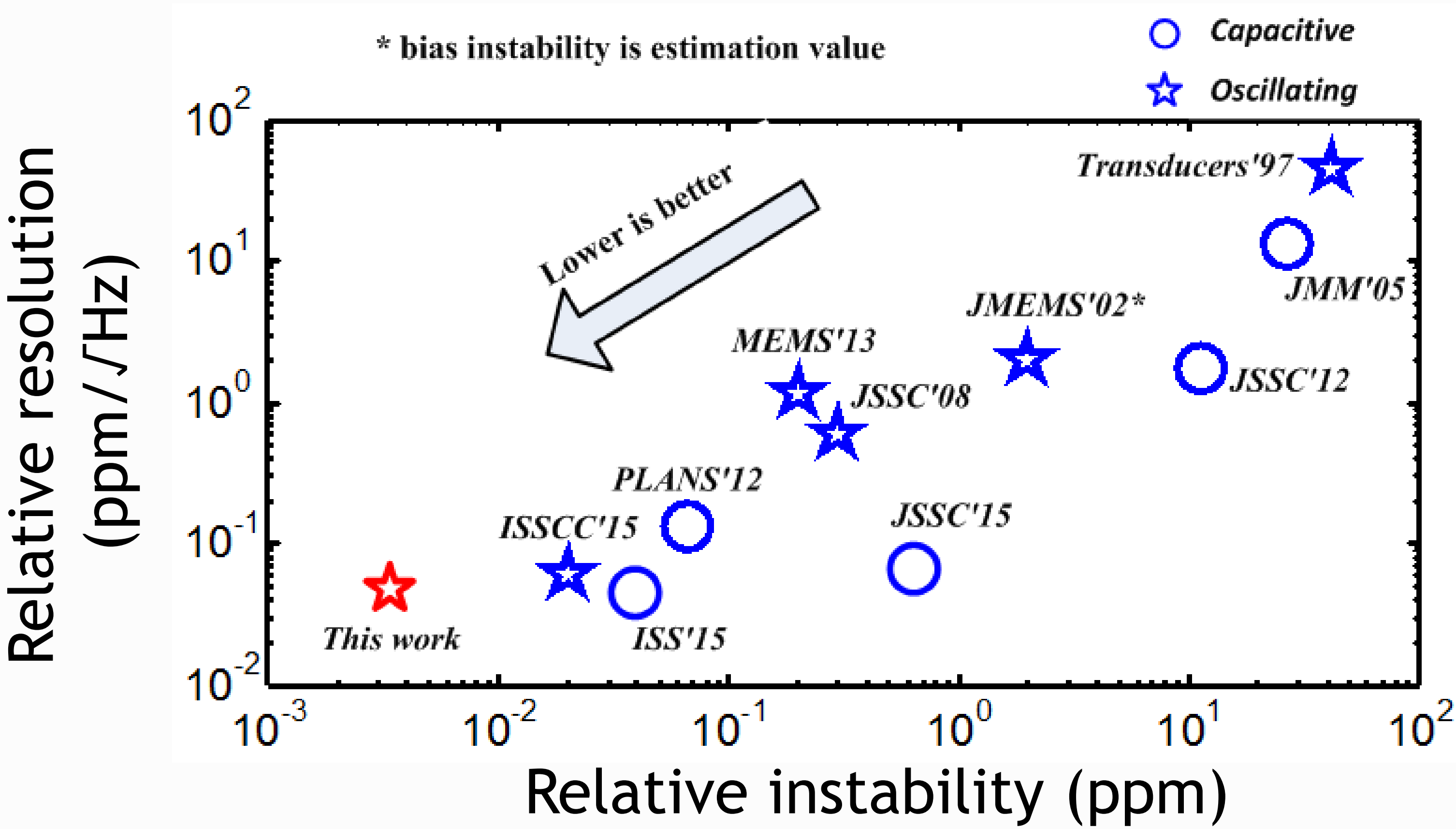
**Relative noise density= noise density / full scale

Performance Comparison (cont.)



- Relative performance
  - Relative resolution = resolution / full-scale
  - Relative bias-instability = bias-instability / full-scale

Summary (5 steps toward a good chip)

- Comprehensive review to find the **key issue（硬骨头）**
- Carefully analysis before entering the design phase, to identify the **key factors**
- Novelty in circuit design to perform beyond the trade-off
- Carefully verification (pre-, post-, / PVT, Monte-carlo) to increase the yield of the design
- Correctly measurement & evaluation

Reminders

- Homework #1
  - Due on May 7th (Expired)
- Homework #2
  - Due on May 21th (Expired)
- Homework #3
  - Due on June 4th
- Project #1
  - Due on June 14th (with a short presentation)
  - Two project proposals (ADC & Two-stage opam)
  - Will have a short presentation