模拟集成电路课程设计（版图）
Layout in Analog Integrated Circuits

Assist. Prof. Jian Zhao
Prof. Guoxing Wang

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Instructors

- **Time**
  - Lecture: Tuesday 14:00 to 15:00
  - Lab: Tuesday 15:00~17:30, Friday 14:00~17:30
- **Lecturer**
  - Assist. Prof. Jian Zhao (赵健) & Prof. Guoxing Wang
  - School of Microelectronics, Room 427
  - zhaojianycc@sjtu.edu.cn
- **Teaching Assistant**
  - Dr. Luo Jing (罗京)
  - School of Microelectronics, Room 404.
  - luojing@sjtu.edu.cn

Syllabus (New)

L1: Introduction

L2: Process, Active & Passive Components

L3: Process variation & Matching Issues

L4: Parasitic Effects

L5: ESD protection, Floorplan & Packaging

L6: Design for Manufacture (Prof. Li Yongfu)

L7: Advanced EDA tools for analog design (Cadence)

L8: Project Review

Review of Lecture #4

- Parasitic effect in IC design
- Parasitic capacitor & crosstalk
- Parasitic resistor & grounding issue
- Parasitic BJT & protection
- Utilize Parasitic effects

Outline of Lecture #5

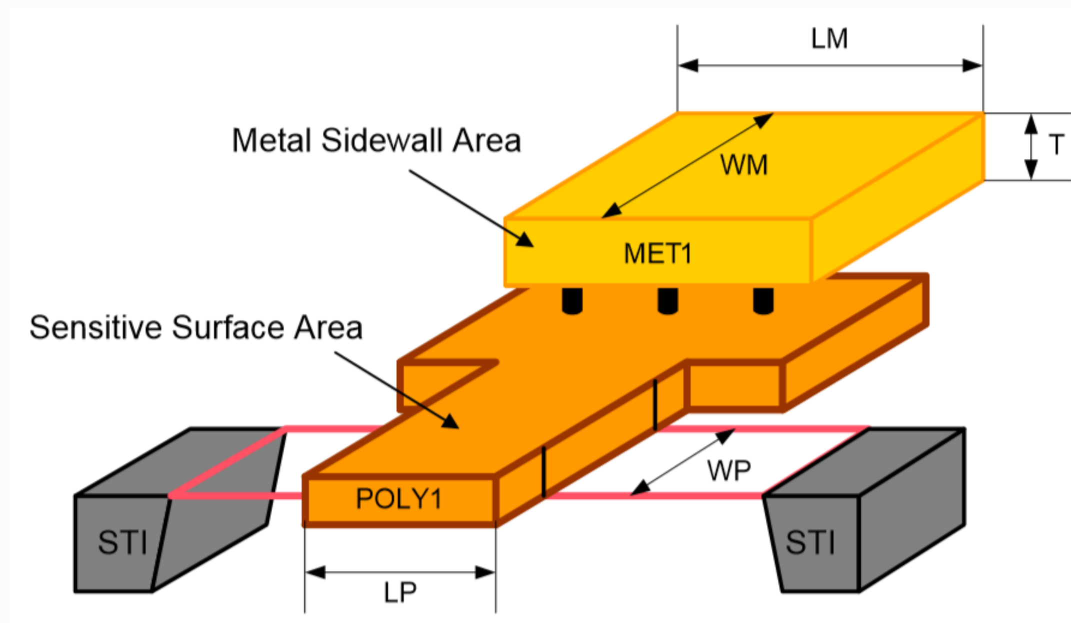
- Two Important Rules Towards a Chip
  - Antenna, off-grid
- ESD Protection & PAD
  - ESD Introduction (Cause+Model+Influence)
  - ESD Protection (Concept+Architecture+Circuits)
- Floorplan
  - Pin-driven, Block-driven, Signal-driven
- Packaging
  - Introduction, Bonding

Antenna Effects

- Influence of Antenna Effect (Gate burnt)
- Plasma induced gate oxide damage

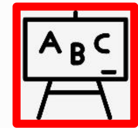
Antenna ration

$$Rx = \frac{P \times T}{WP \times LP} = \frac{Metal Sidewall Area}{Sensitive Surface Area}$$



Antenna Effects

- Influence of Antenna Effect (Gate burnt)
- Plasma induced gate oxide damage
- **Solution: Jumper, Diode (parasitic, intentional)**

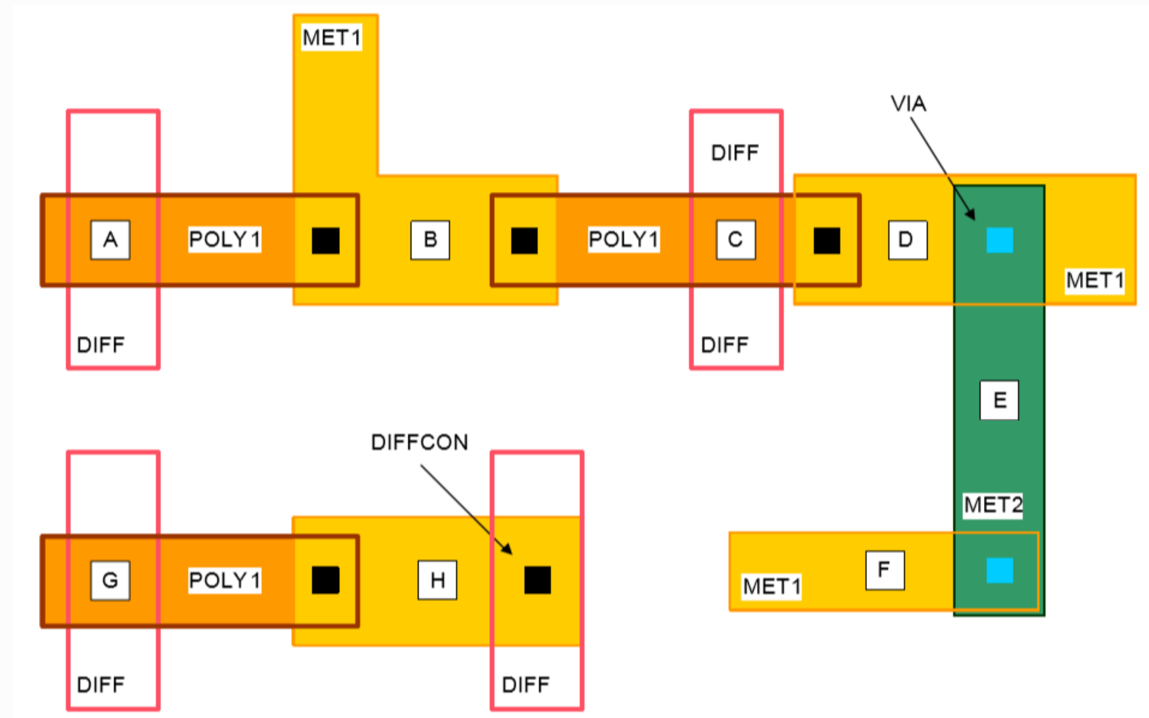


Antenna ration: Metal #1

$$\frac{area(B+D)}{area(A+C)}$$

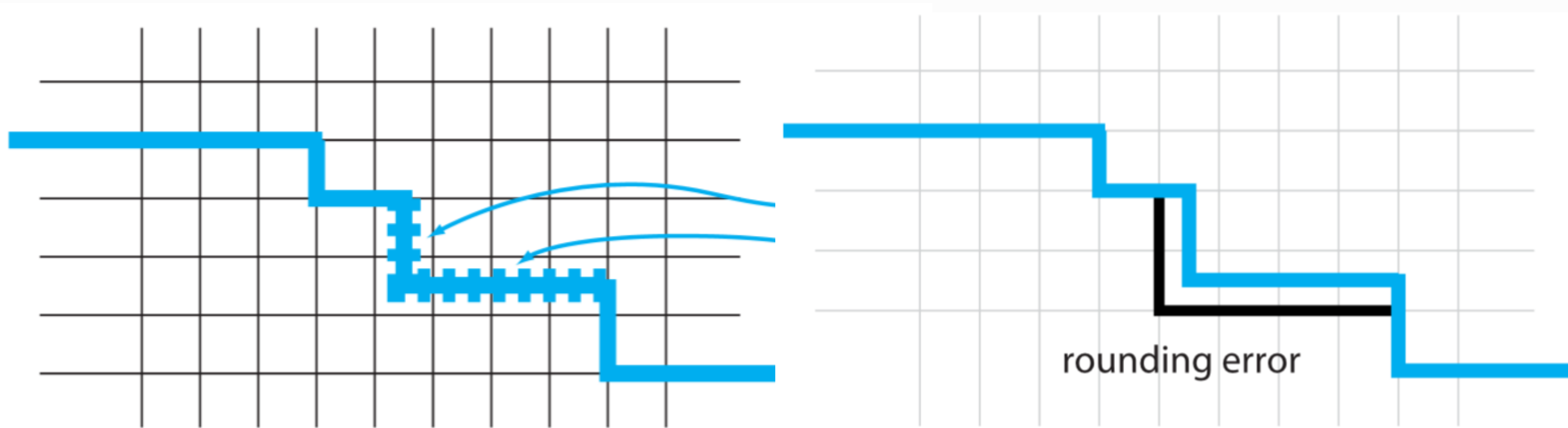
Antenna ration: Metal #2

$$\frac{area(E)}{area(A+C)}$$



Data format & off-grid

- Data format (GDS-II)
- Off-grid violation & rounding error
- Off-grid induced failure



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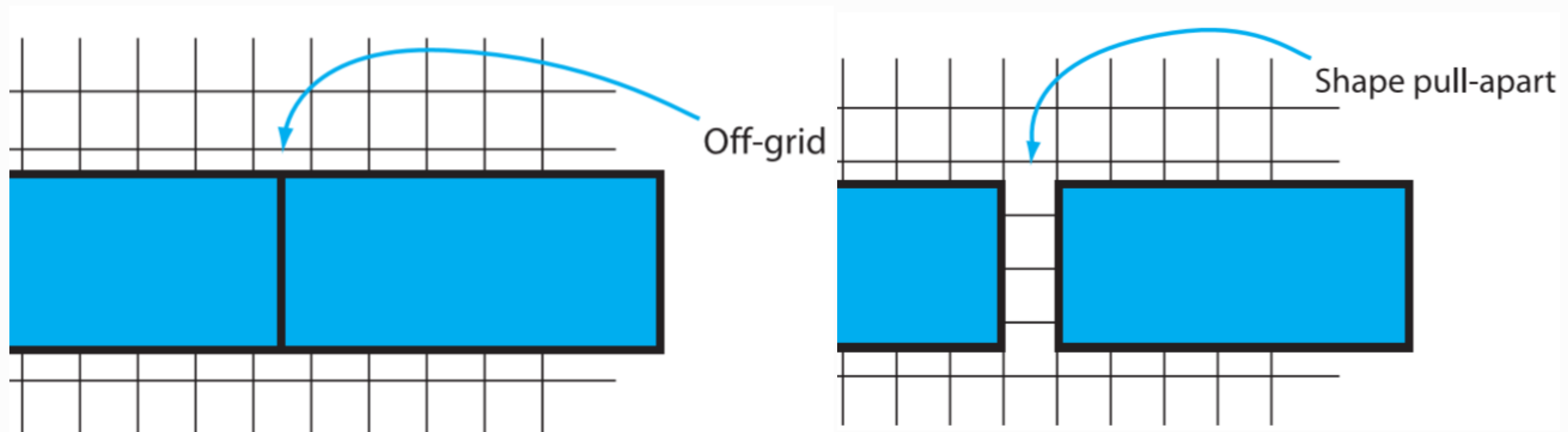

Outline of Lecture #5

- Two Important Rules Towards a Chip
  - Antenna, off-grid
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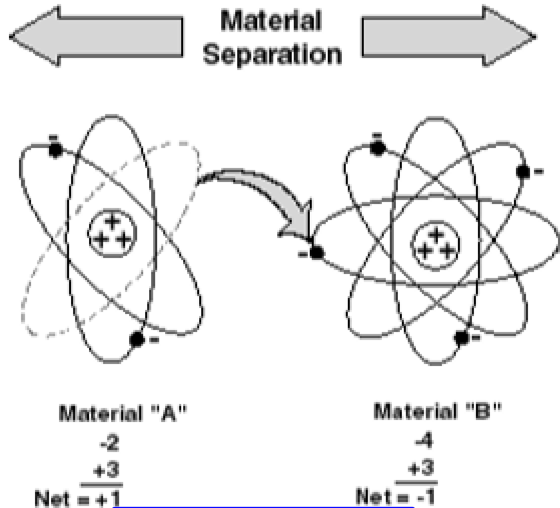
Principle of ESD

- Triboelectric charging happens when 2 materials come in contact and then are separated.
- An ESD event occurs when the stored charge is discharged.

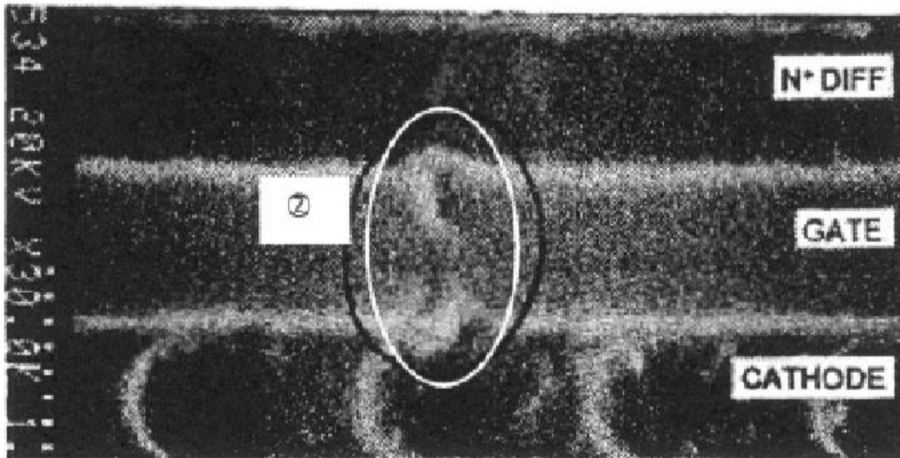


Charge

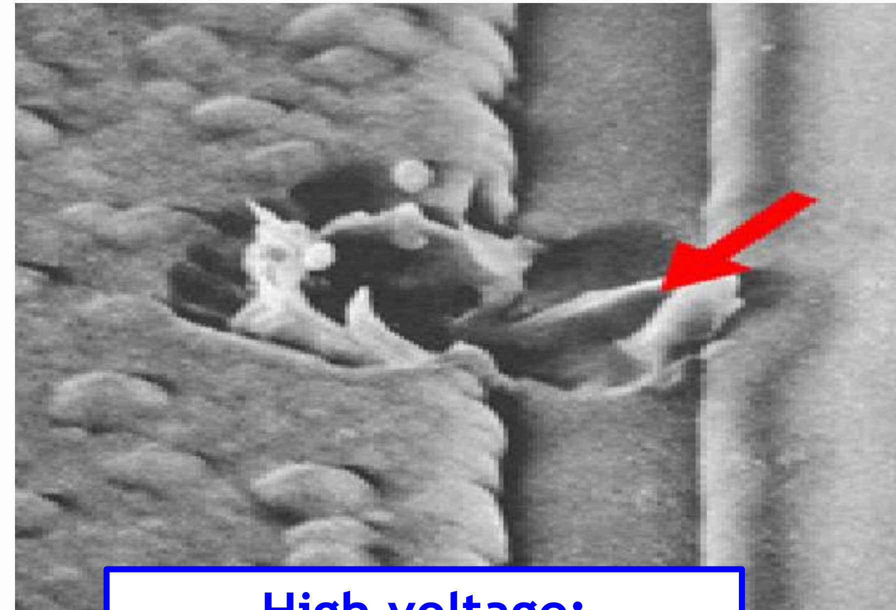
Discharge

Motivation of ESD (静电放电)

- Electrostatic Discharge (ESD) is responsible for up to 70% of failures in semiconductor industry
- An ESD event creates high currents and electric fields in semiconductor devices



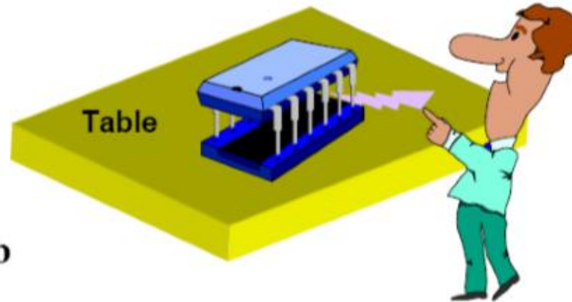
High current:
Joule heating melt

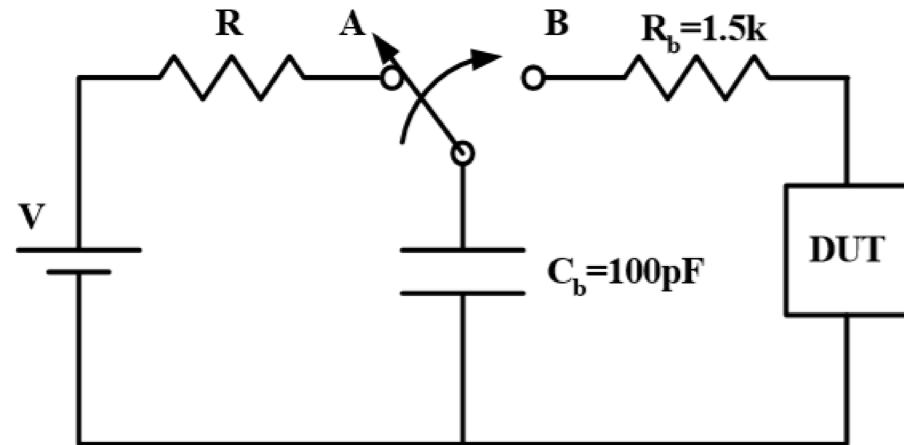


High voltage:
Dielectric breakdown

Model for ESD event

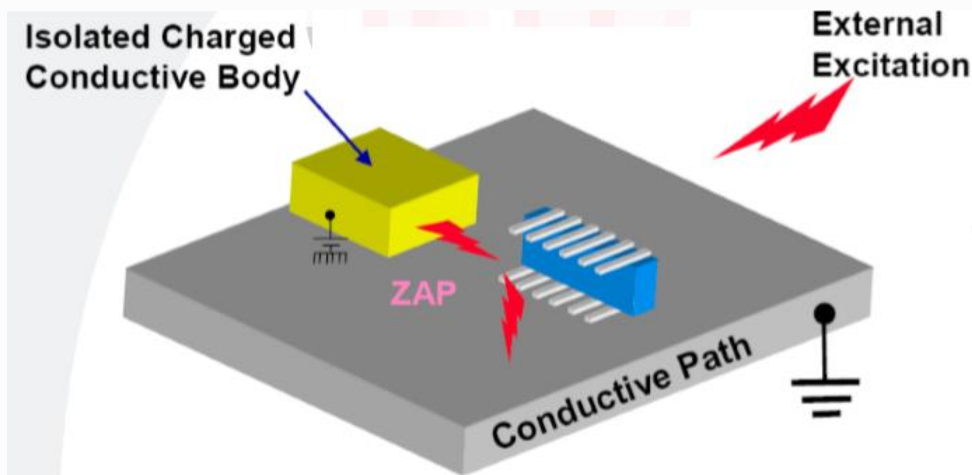
- Human body model (HBM)
  - Mimics the human touching of the DUT
  - Voltages as high as 10kV
  - Human body modeled by R_b= 1.5kΩ, C_b= 100pF
- Machine model (MM)
- Charge device model (CDM)

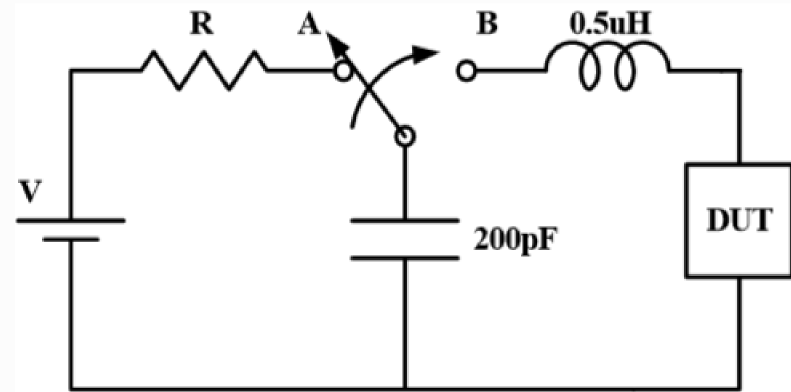




Model for ESD event

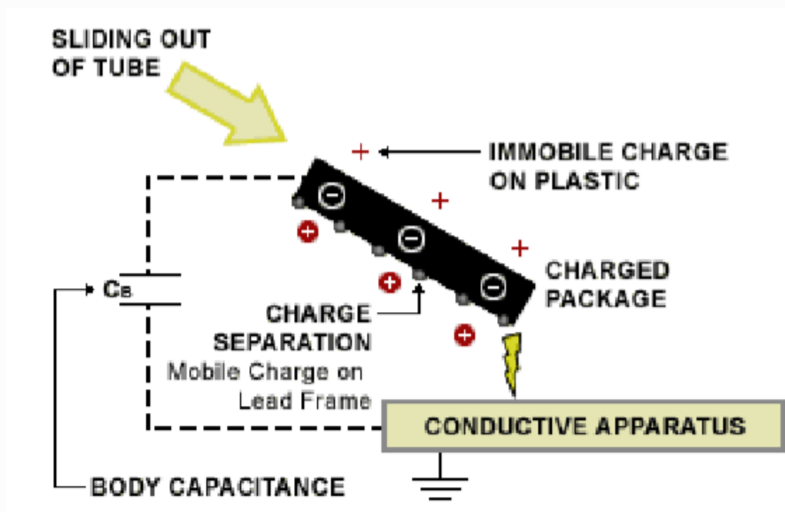
- Human body model (HBM)
- Machine model (MM)
  - Mimic the damage caused by charged machine
  - Voltages as high as 100-500V can be generated
  - Machine modeled by C= 200pF, L= 0.5μH,
- Charge device model (CDM)

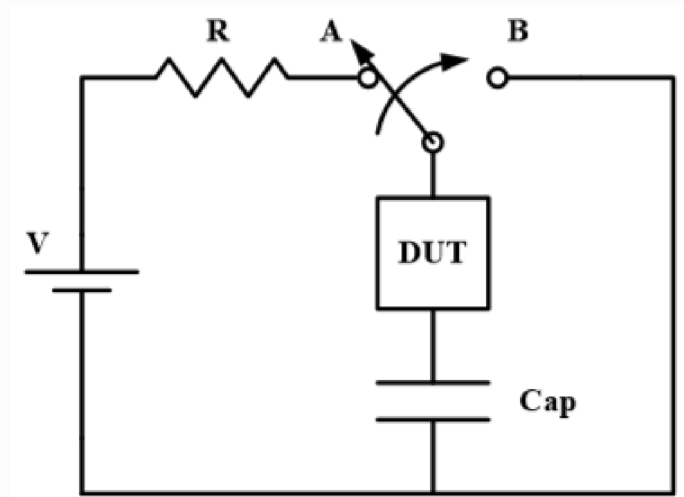




Model for ESD event

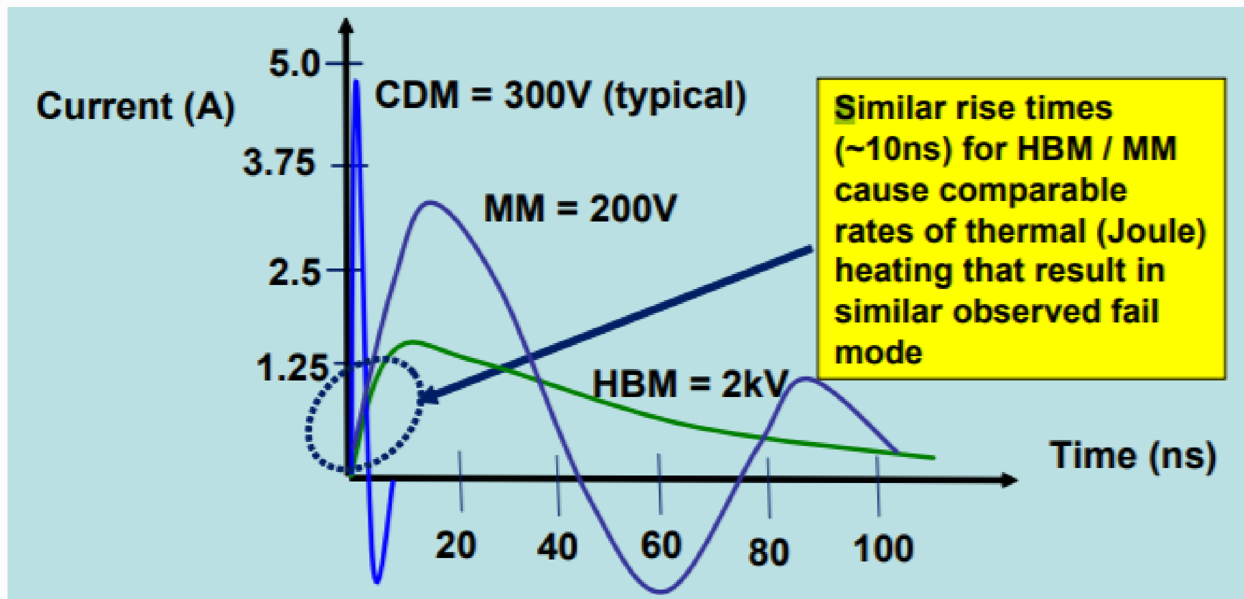
- Human body model (HBM)
- Machine model (MM)
- Charge device model (CDM)
  - Discharge event between charged DUT and ground
  - Modeled by Capacitor (Cap) in series with DUT
  - Total Capacitance (Cap) is dependent

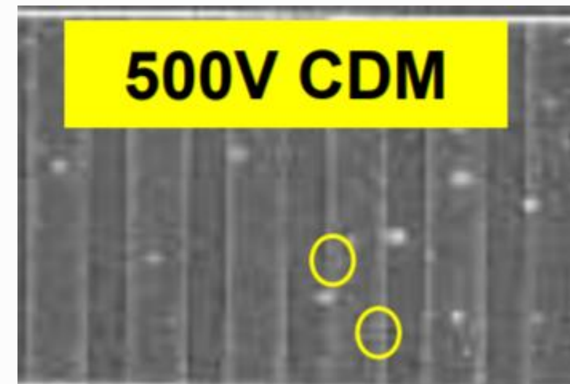




Comparison between three models

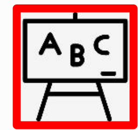
- HBM rise time ~ 2-10ns, decay time 130-170ns
- CDM very high amplitude , occurs for 500ps-1000ps
- MM is discontinuing used (same damage, same principle to CDM)





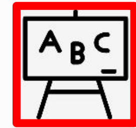
Objective of ESD protection

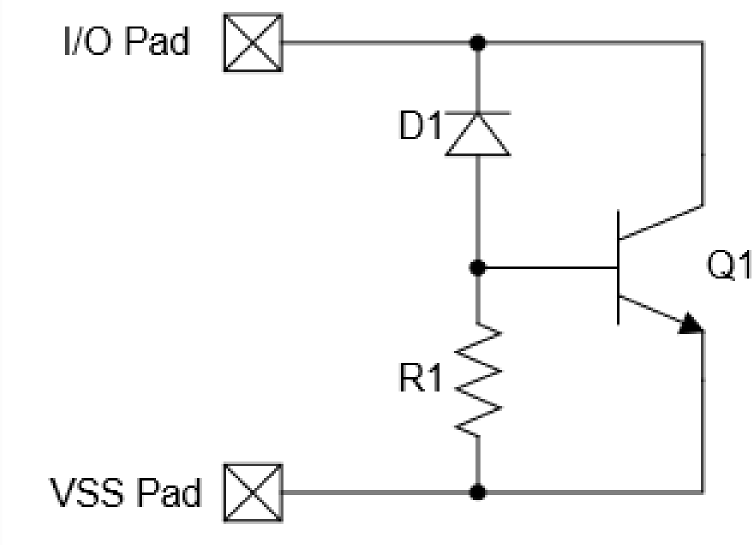
- Protect both the internal circuits and ESD device during discharge (Any two pads!!!)
- Minimize layout area without degrading ESD protection level
- Ensure high signal quality through I/O (Performance)
- High latch-up immunity of CMOS IC's
- CMOS compatible (Low cost)



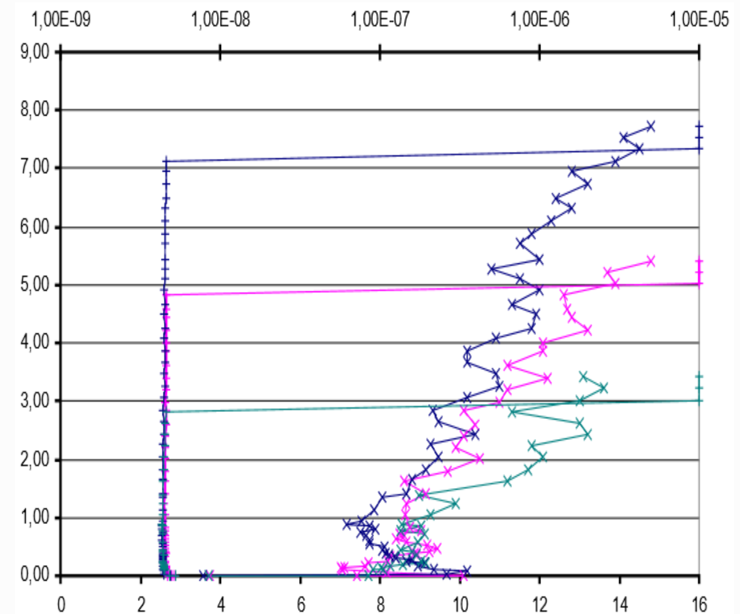
Basic ESD protection circuits

- Non-breakdown based ESD circuits
  - BJT/MOSFET clamp, Diode (forward biased)
- Breakdown base ESD circuits
  - ggNMOS, gcNMOS, TFO (Thick field oxide), SCR





Schematic



I-V Curve (V, A)

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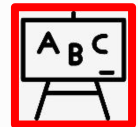
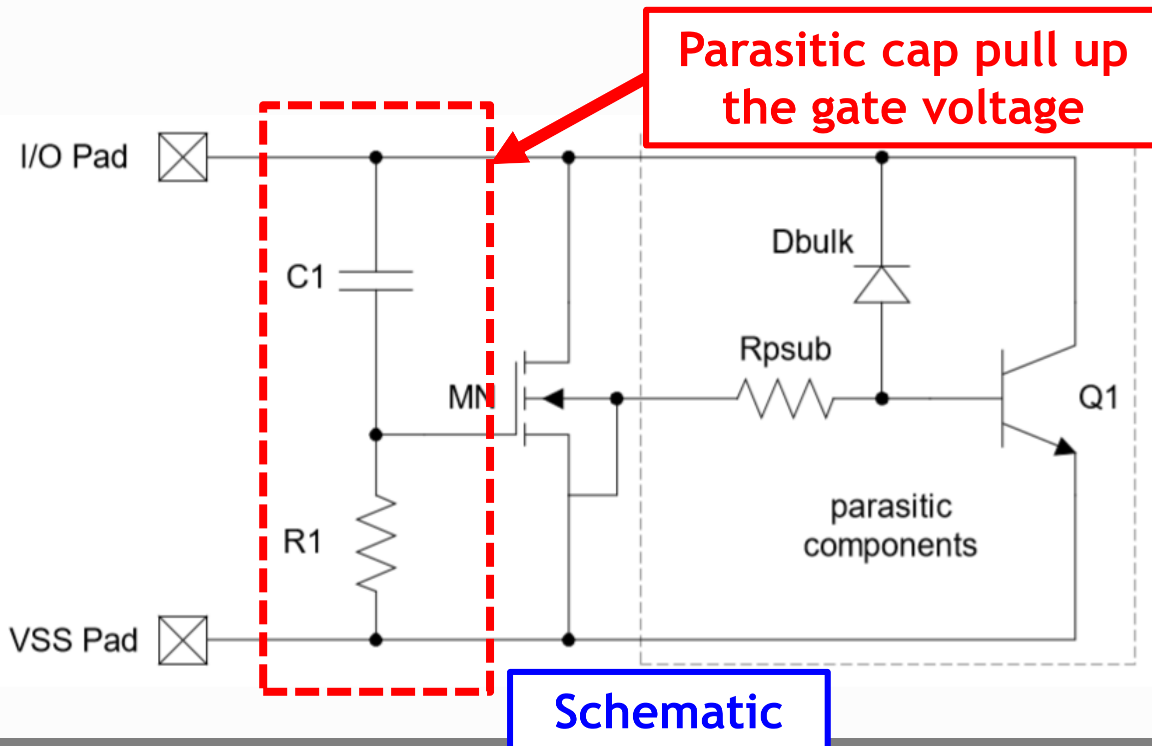


Parasitic cap pull up the gate voltage



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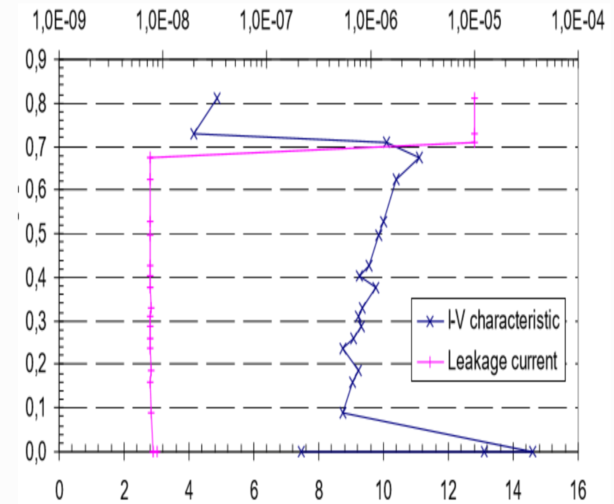

I-V Curve

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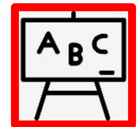

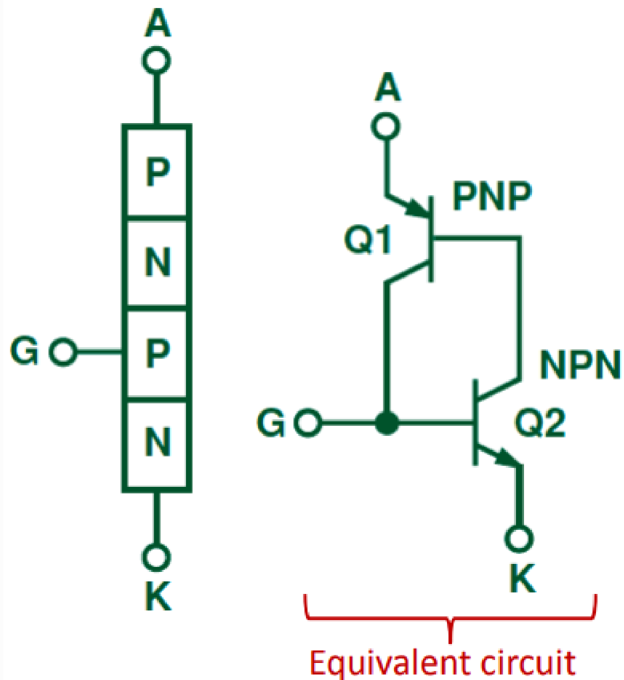

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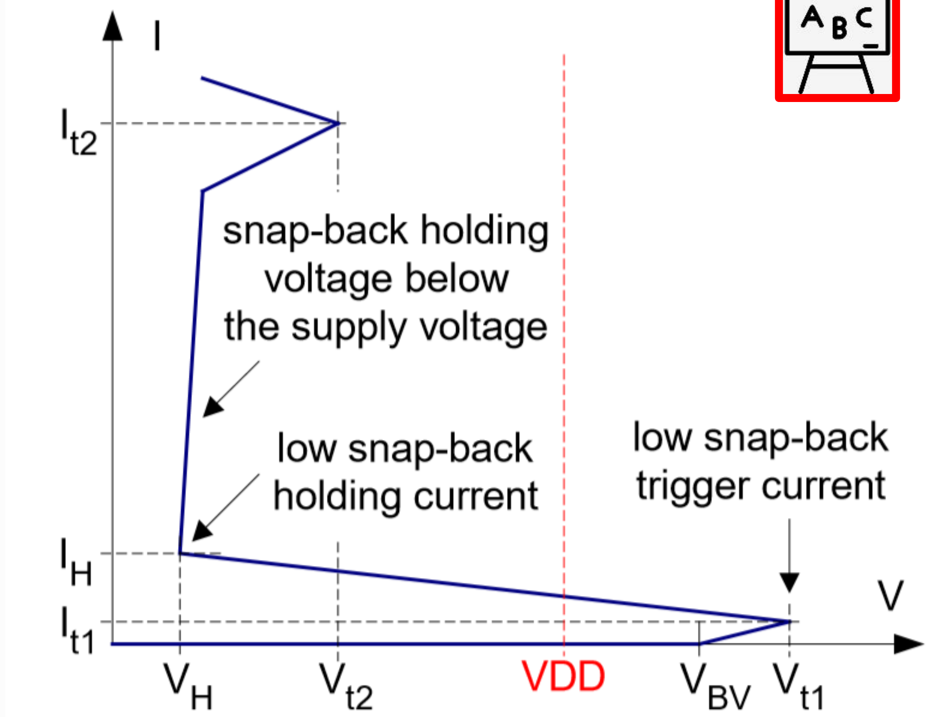
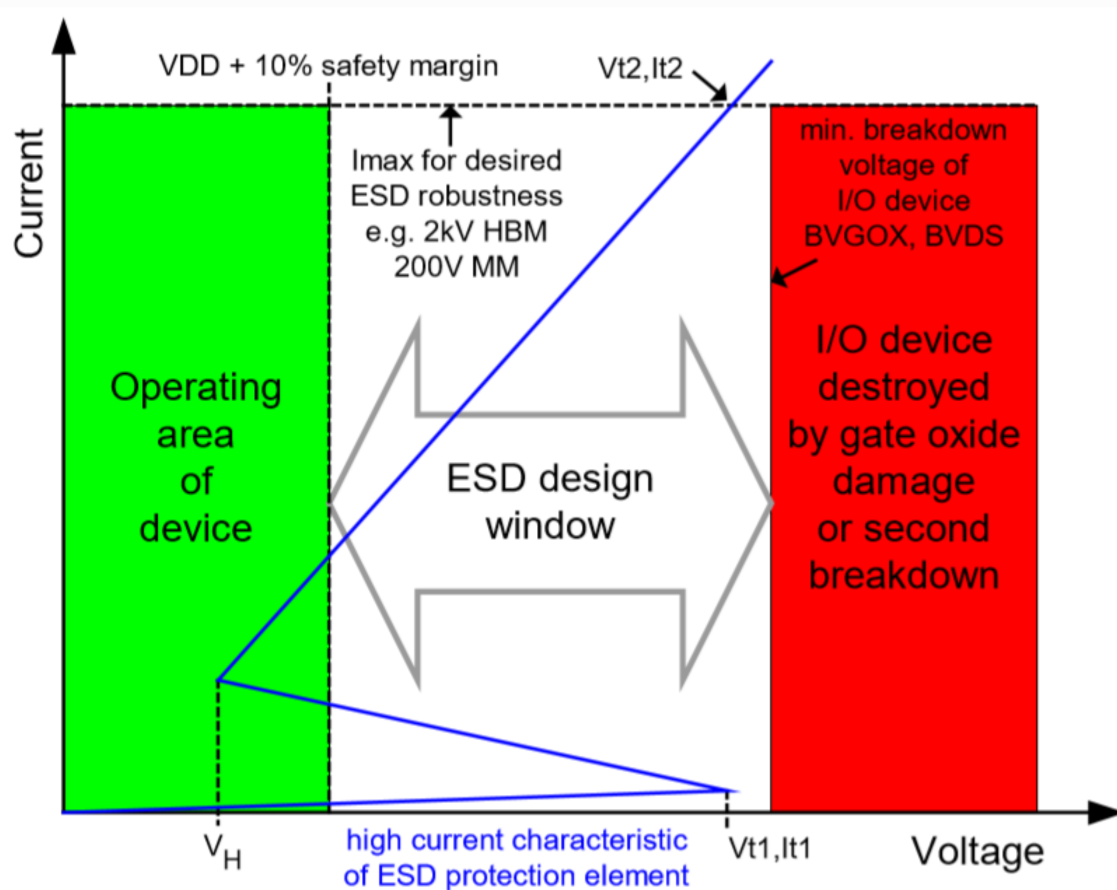


I-V Curve

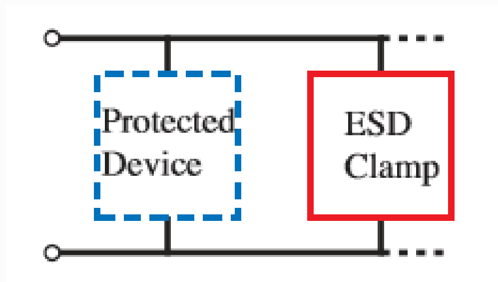
ESD Design window

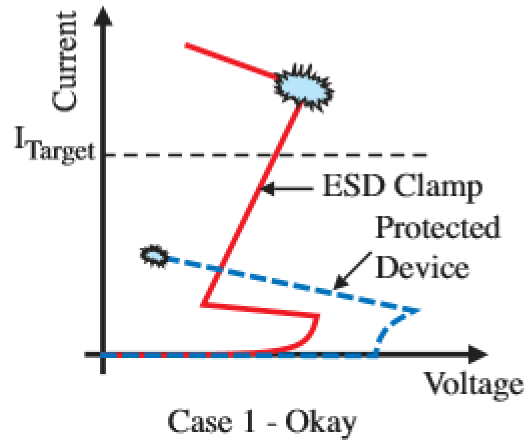
- Two critical point should be within the design window
  - (Vt1, It1), (Vt2, It2)

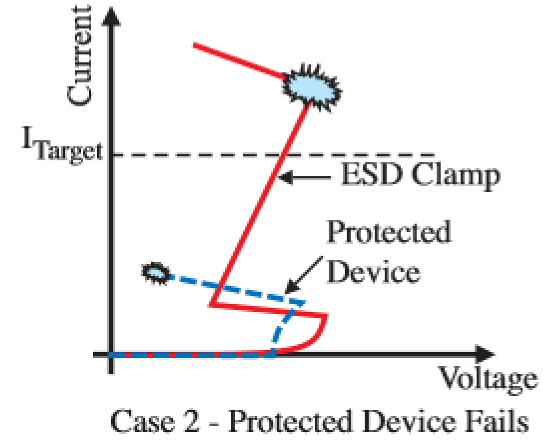


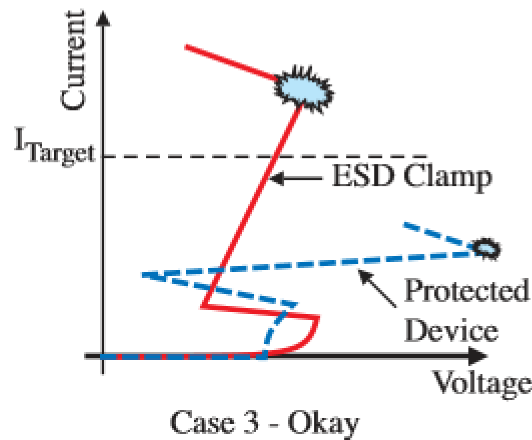
ESD Design window

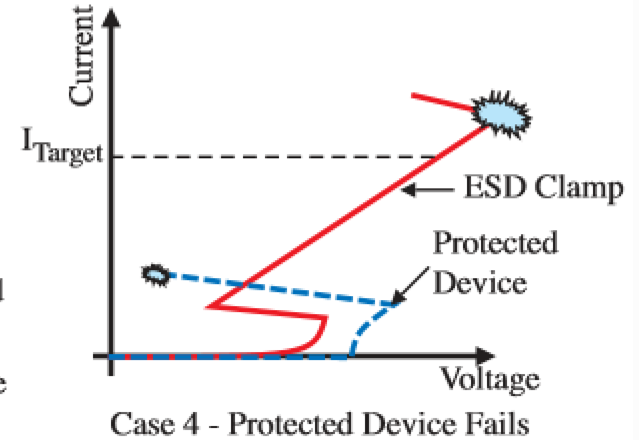
- Goal: Sink the ESD current and clamp the voltage.





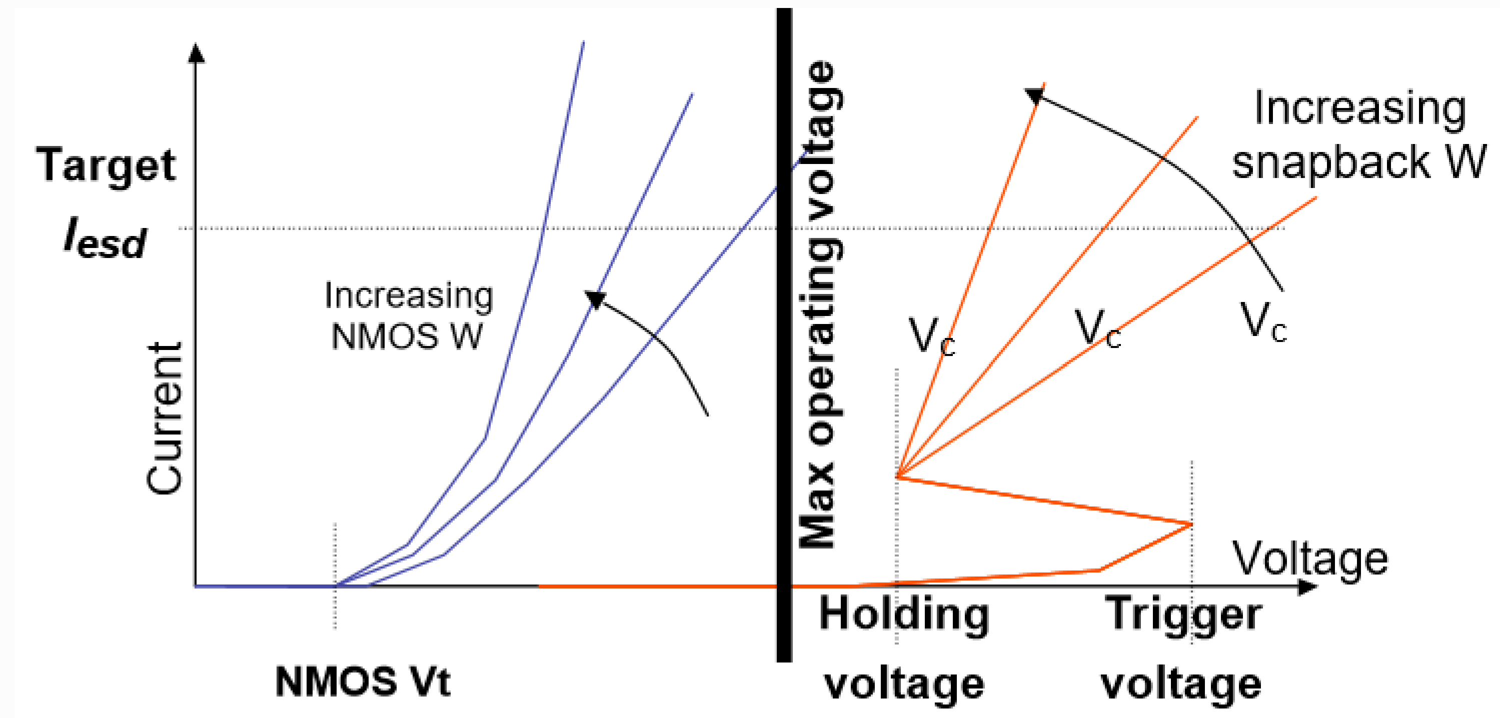






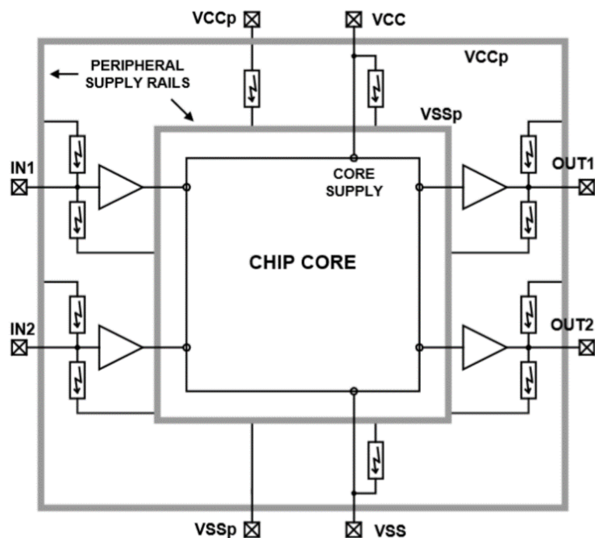
Key parameters in ESD circuits

- Comparison Between the Turn-on and the Snap-back Clamp
  - Increasing the width of the clamp will reduce the clamp voltage.

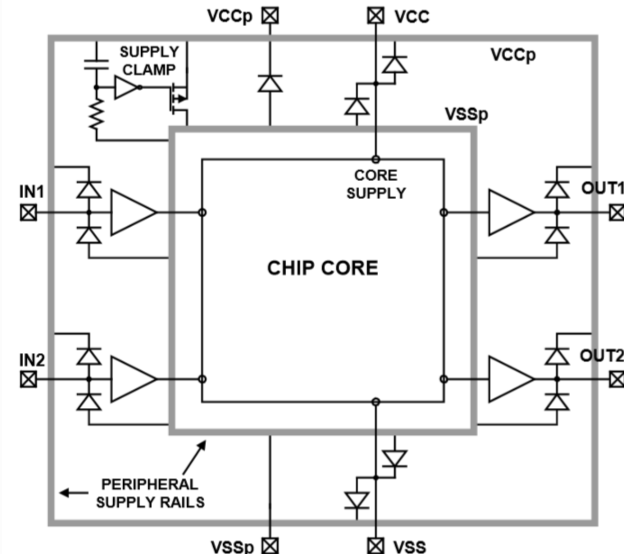


ESD protection strategy

- PAD based protection:
  - Relies on ESD protection devices between the I/O pad and the ground rail, **forward biased** or **break down**
- Power rail based protection:
  - Dual diodes for I/O pad (**forward biased**) + Strong supply clamp



PAD based protection



Power rail based protection

Outline of Lecture #5

- Two Important Rules Towards a Chip
  - Antenna, off-grid
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  - ESD Introduction (Cause+Model+Influence)
  - ESD Protection (Concept+Architecture+Circuits)
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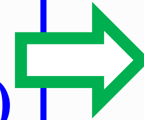
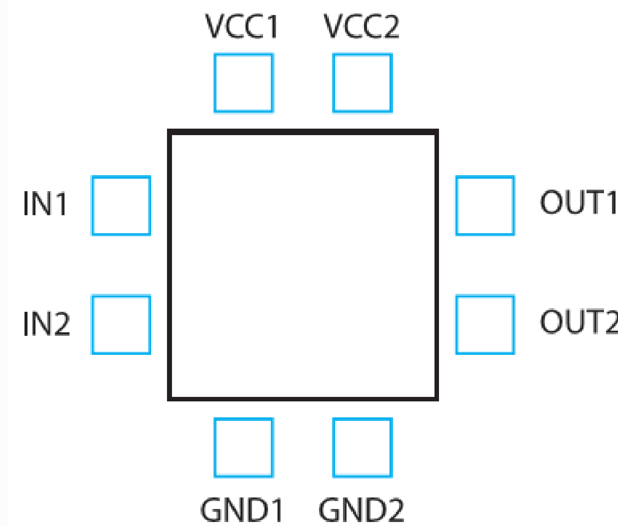
Floorplan (布局)

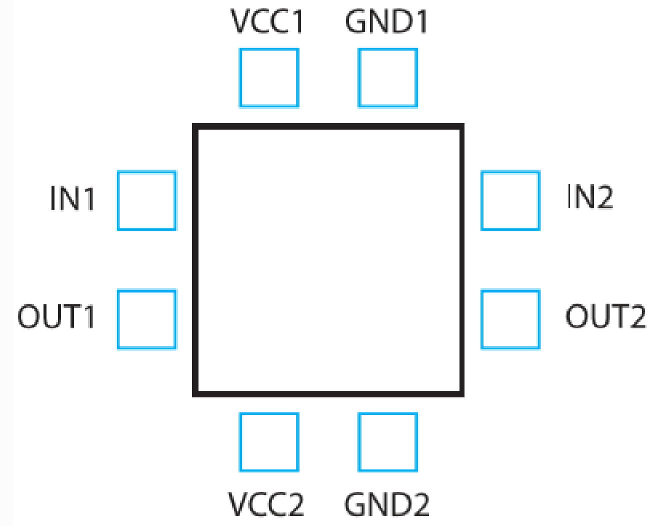
- Pin driven (I/O driven, ESD constraints)
- Block driven
- Signal driven (schematic inspired layout)

Targets: 1. short wire length; 2. less overlaps; 3. Concision (For test and debug)



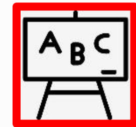
Good looking

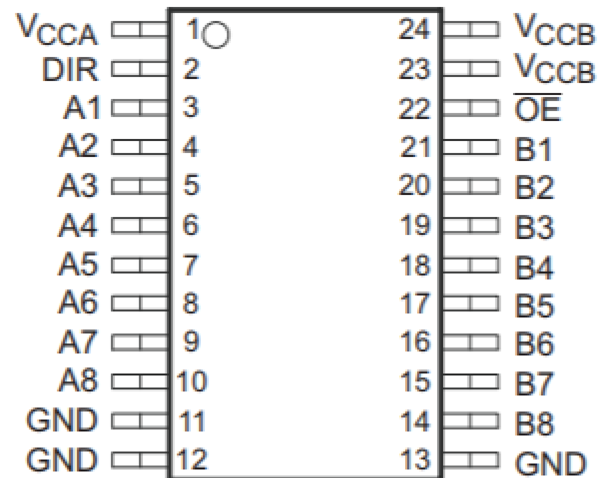




Floorplan

- Pin driven (I/O driven, ESD constraints)
- Block driven
- Signal driven (schematic inspired layout)



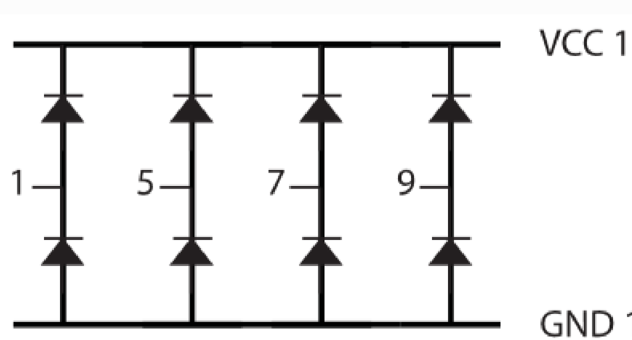


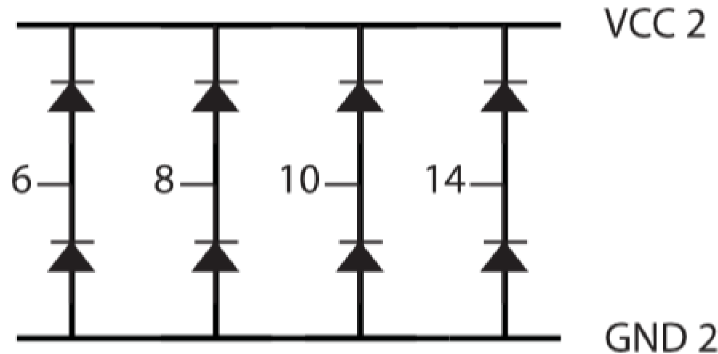
2-channel opam by ADI

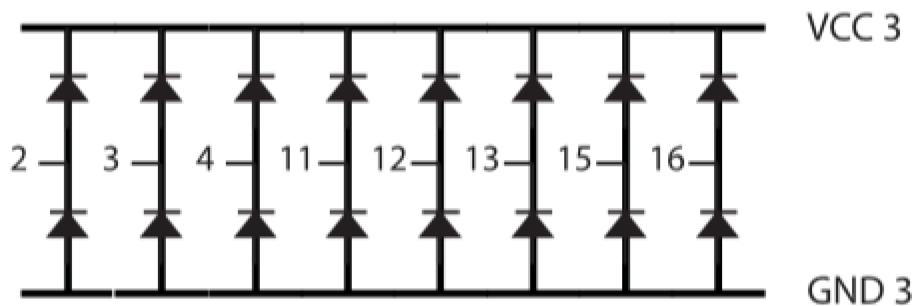
8-channel Level-shifter by TI

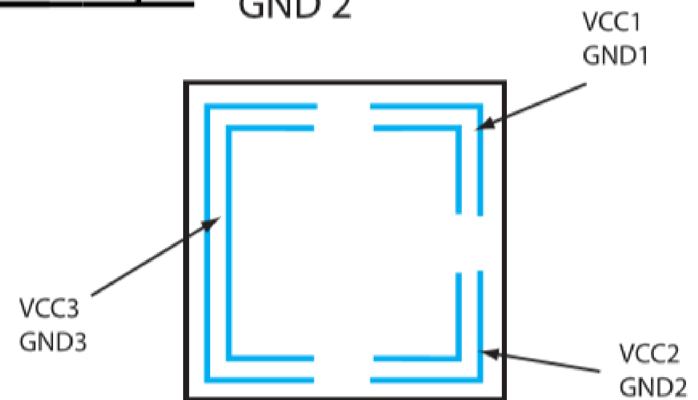
Floorplan

- Pin driven (I/O driven, ESD constraints)
- Block driven
- Signal driven (schematic inspired layout)



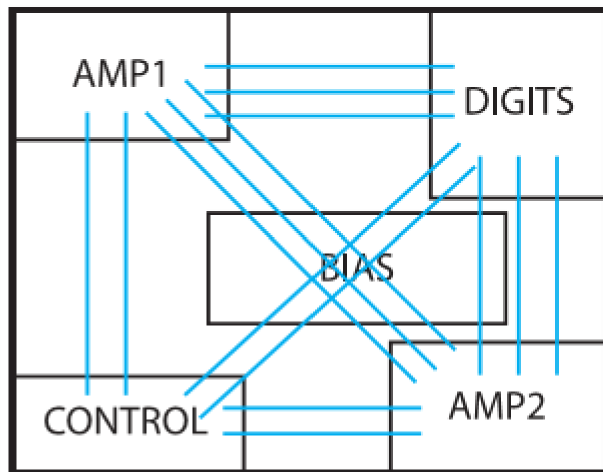




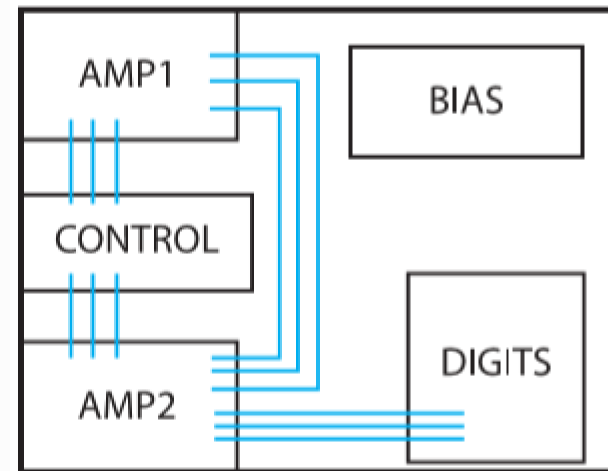


Floorplan

- Pin driven (I/O driven, ESD constraints)
- Block driven
- Signal driven (schematic inspired layout)



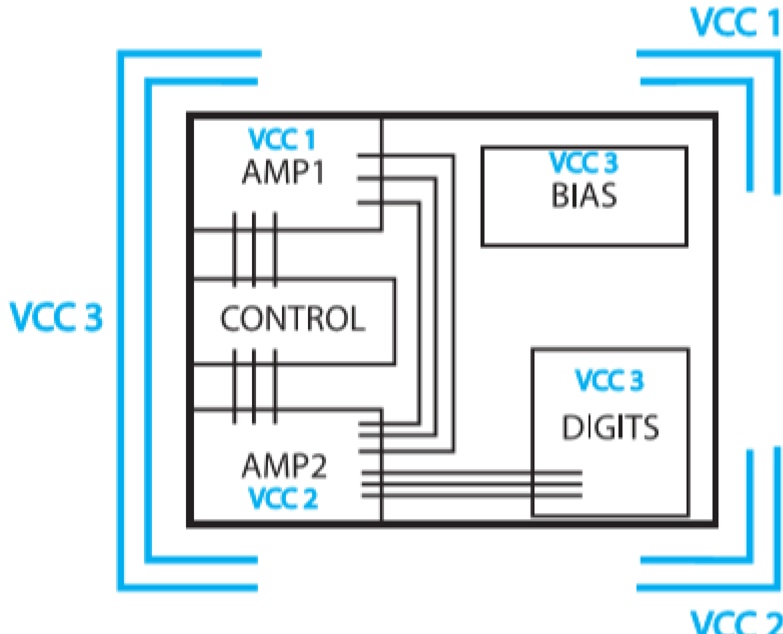
Bad design
(crosstalk out of control)



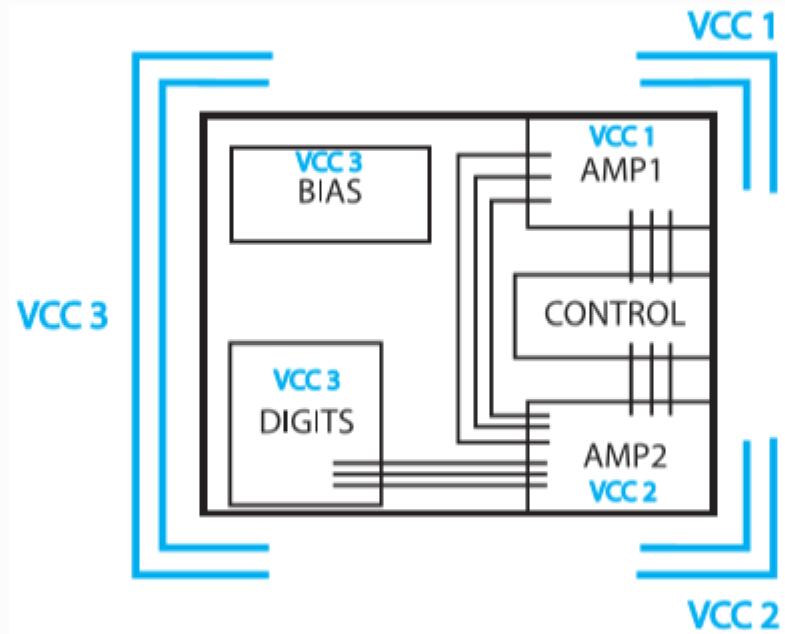
Good design
(crosstalk controlled)

Floorplan

- Pin driven (I/O driven, ESD constraints)
- Block driven
- Signal driven (schematic inspired layout)



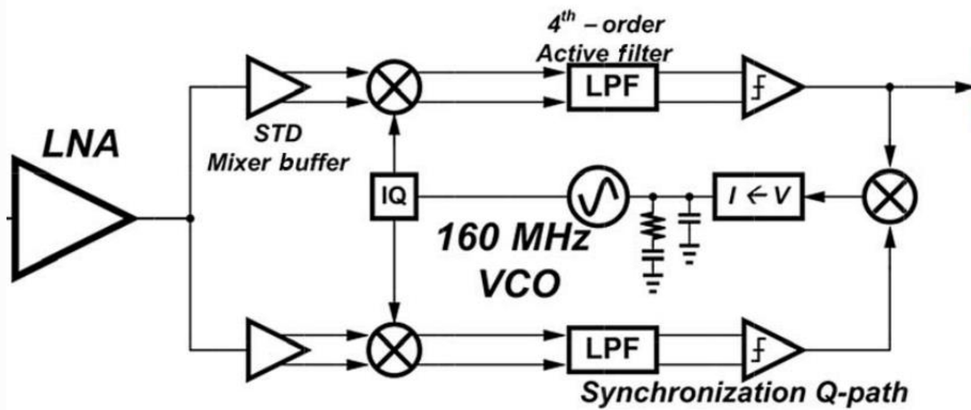
Bad design
(PIN & Block not aligned)



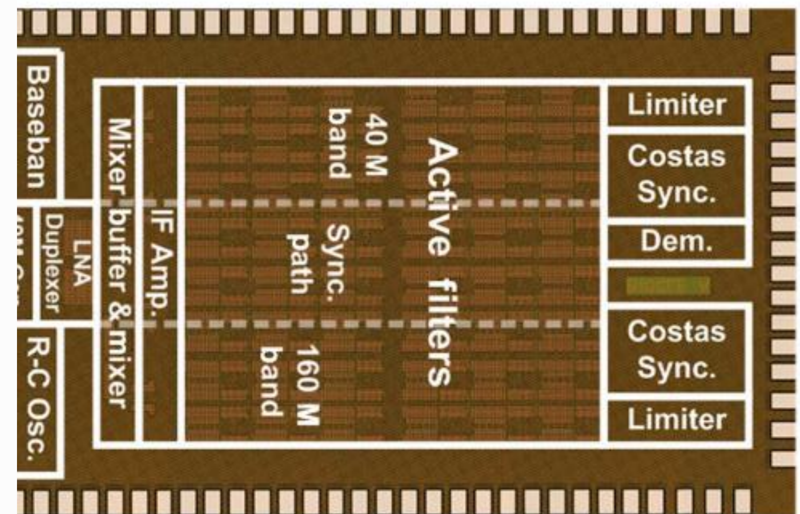
Good design
(Blk & Pin co-design)

Floorplan

- Pin driven (I/O driven, ESD constraints)
- Block driven
- Signal driven (schematic inspired layout)



Schematic



Layout

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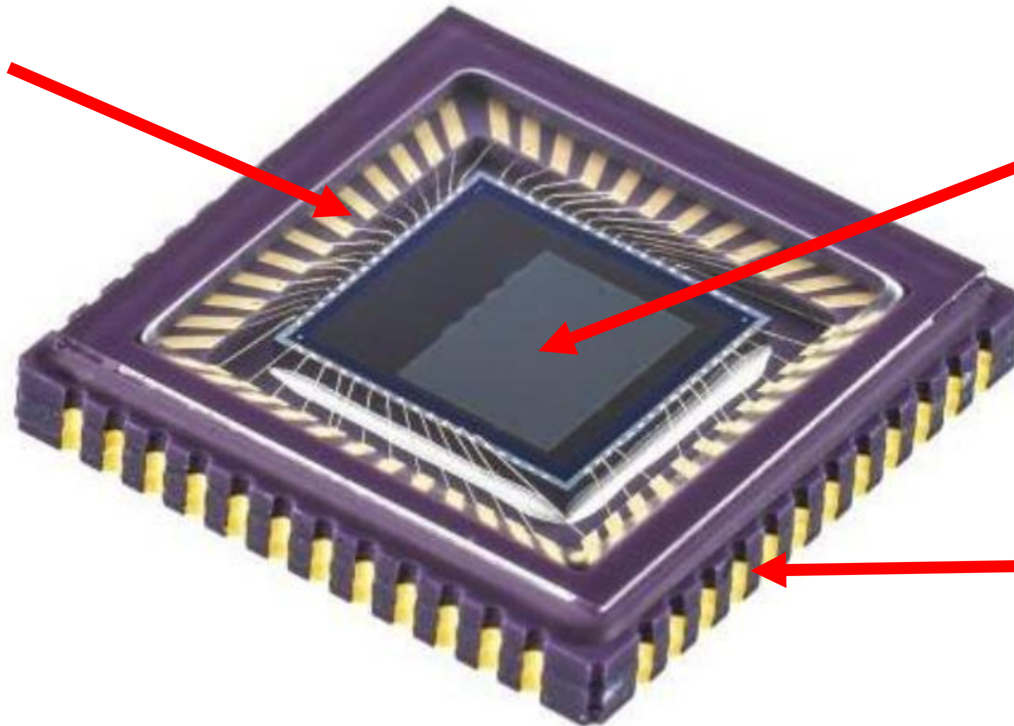
Packaging (Introduction)

- Internal Pads vs. External Pads
  - Internal for Chips
  - External for PCBs

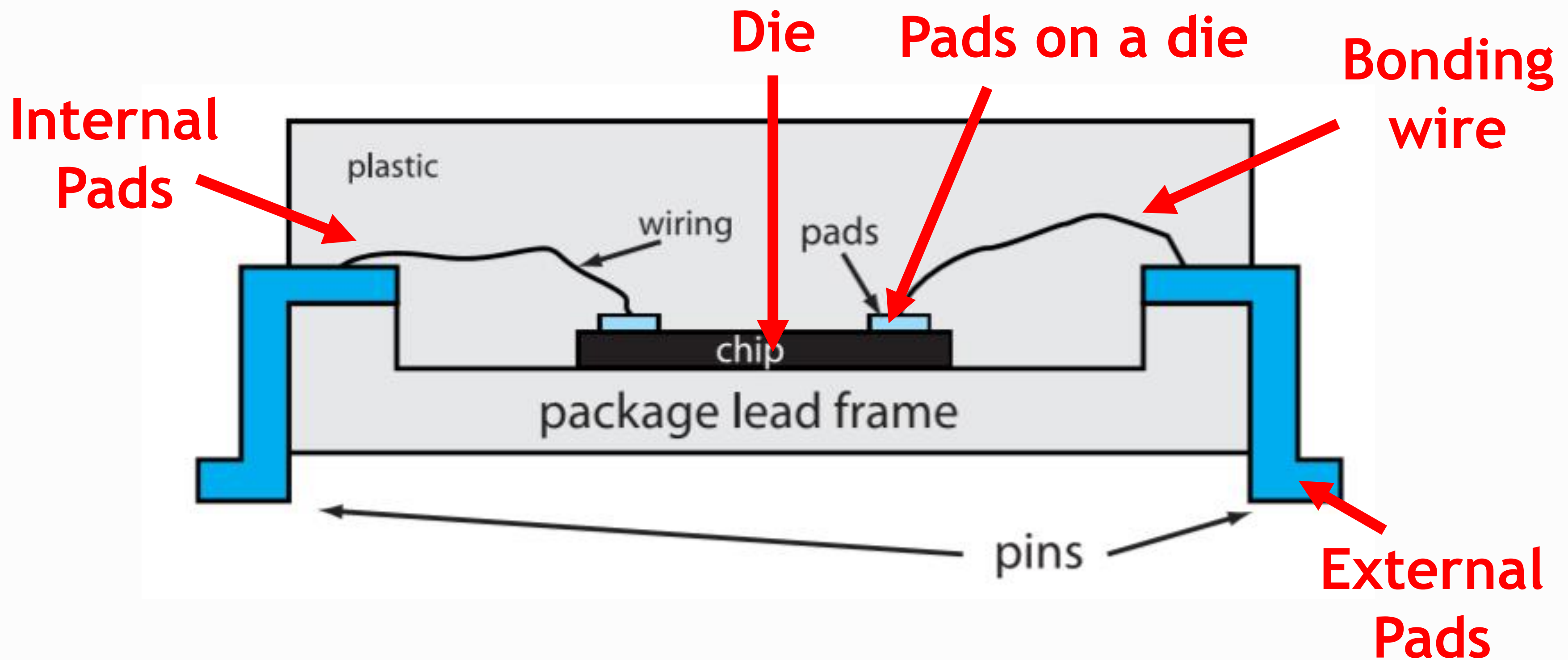
Packaging is also high cost!



Packaging (Introduction)

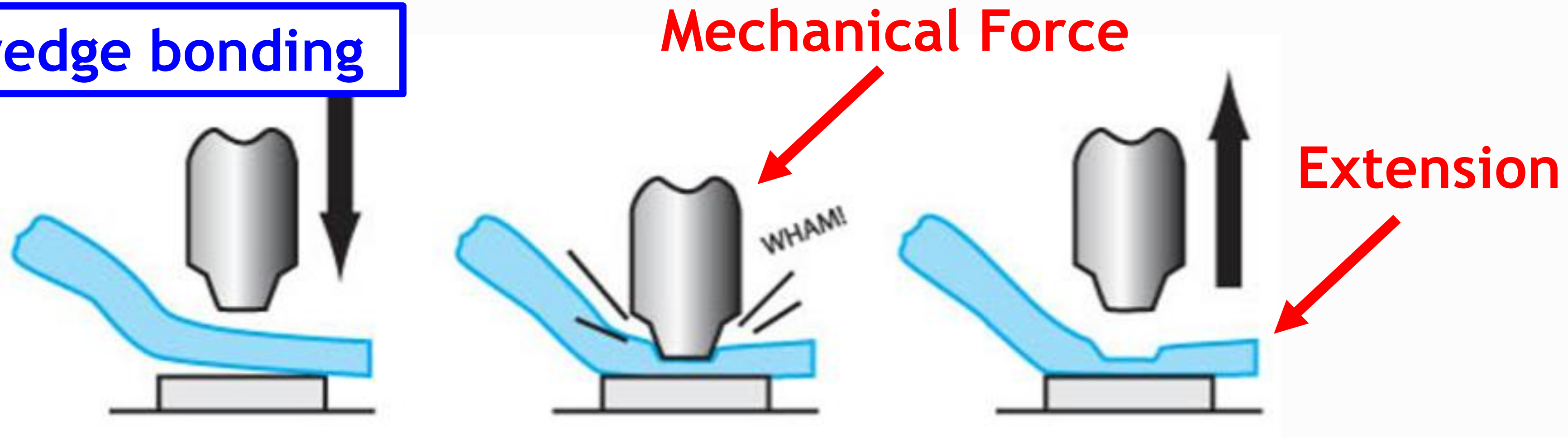
- Internal Pads vs. External Pads
  - Internal for Chips
  - External for PCBs

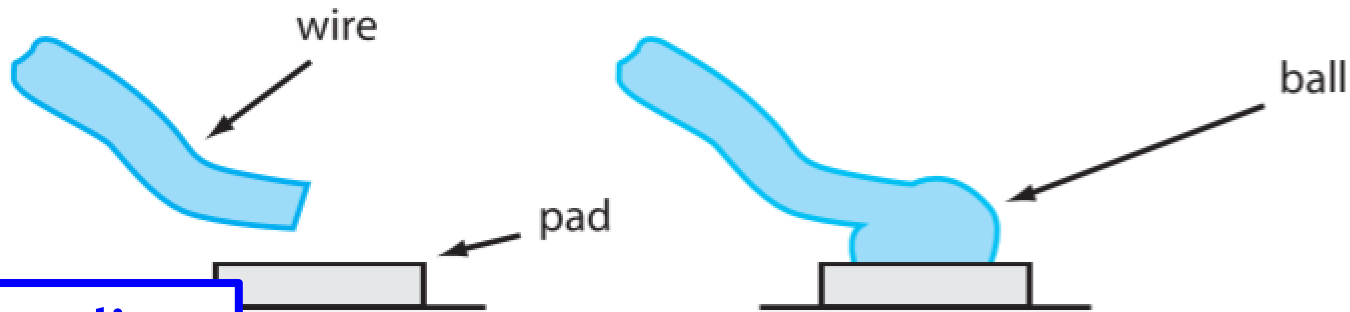
Lateral View!



Packaging (Bonding)

- Ultrasonic wedge bonding /Ultrasonic ball bonding
- Flip chip technology/Multi-tier packaging

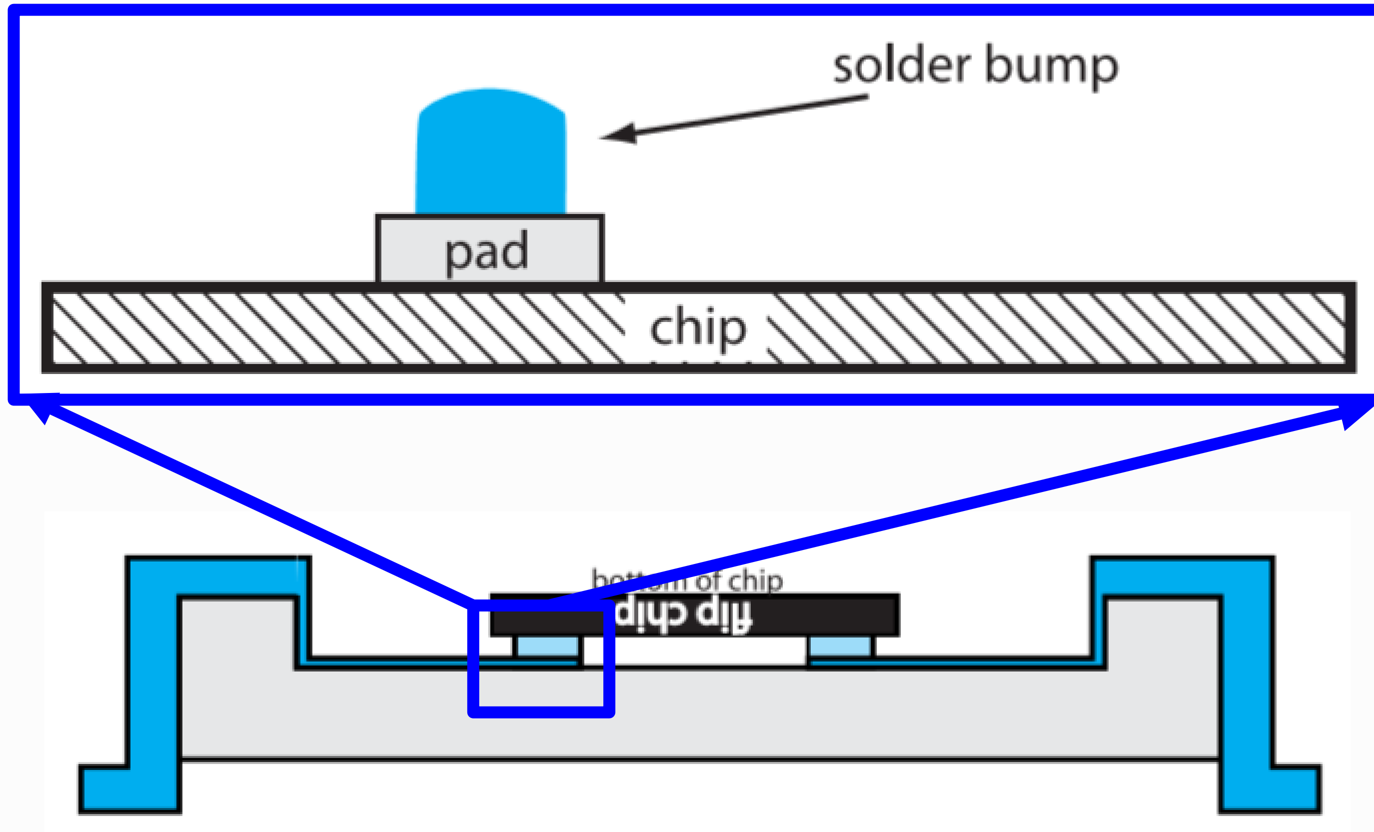




Ball bonding

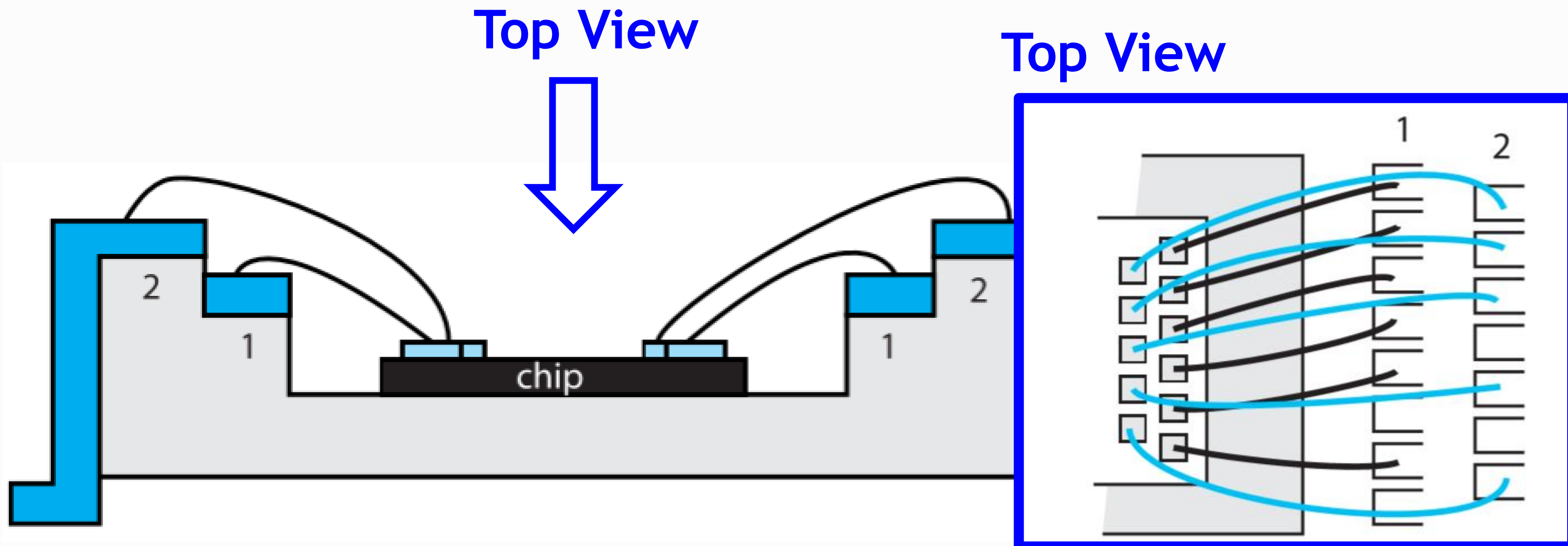
Packaging (Bonding)

- Ultrasonic wedge bonding/Ultrasonic ball bonding
- Flip chip technology (倒装)/Multi-tier packaging



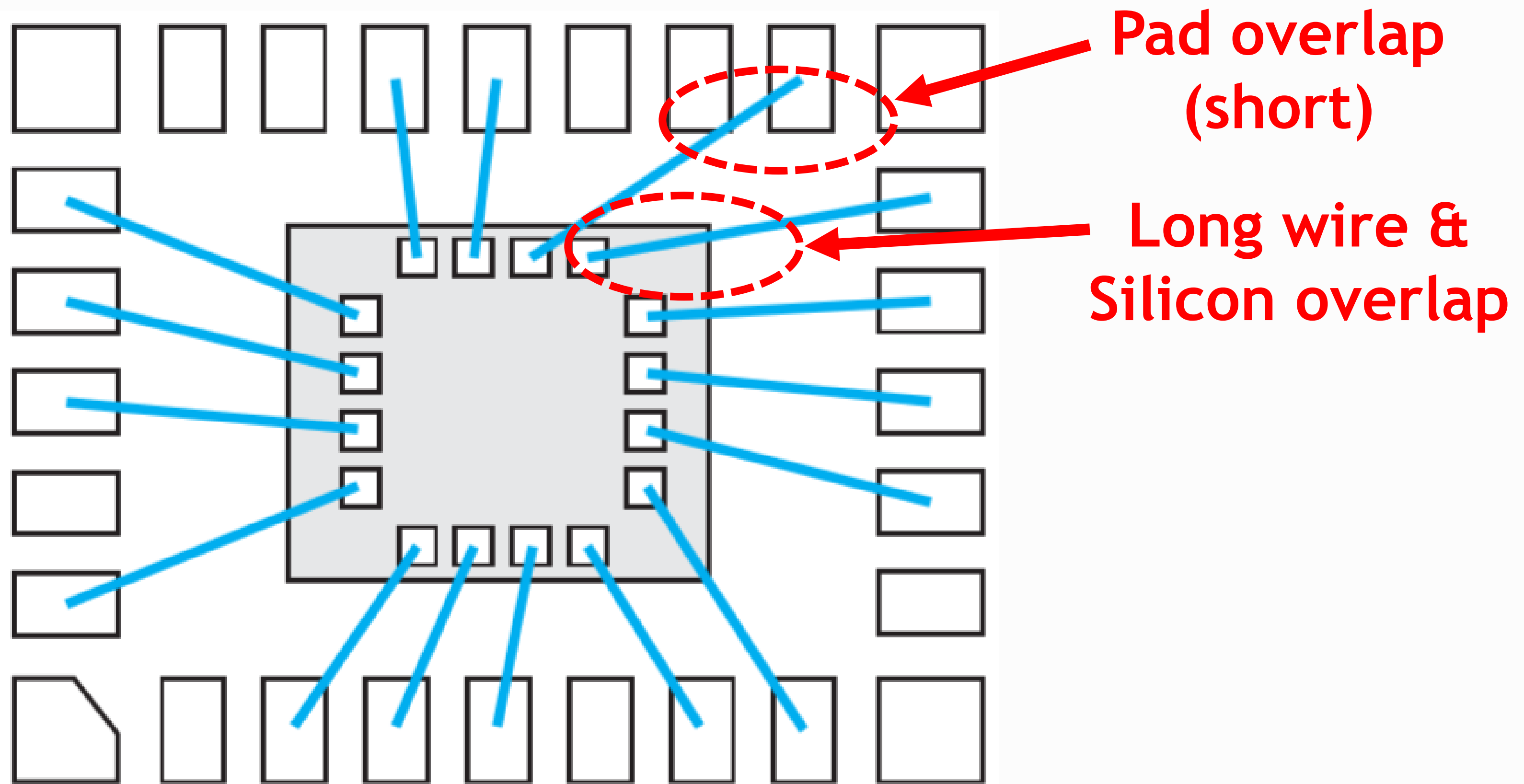
Packaging (Bonding)

- Ultrasonic wedge bonding/Ultrasonic ball bonding
- Flip chip technology/Multi-tier packaging



Packaging (Bonding)

- Bonding with good looking usually performs well
- 45 degree/ Minimum silicon overlap/ Short Wire

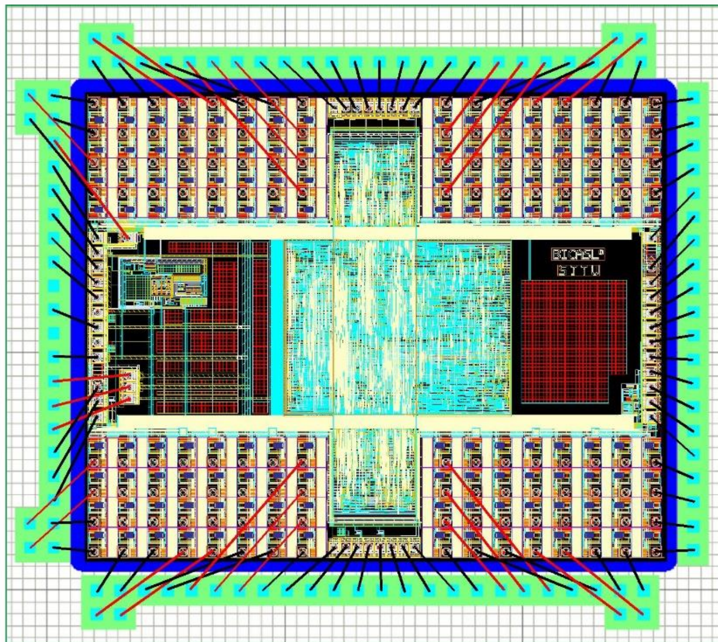


Packaging (Technical files)

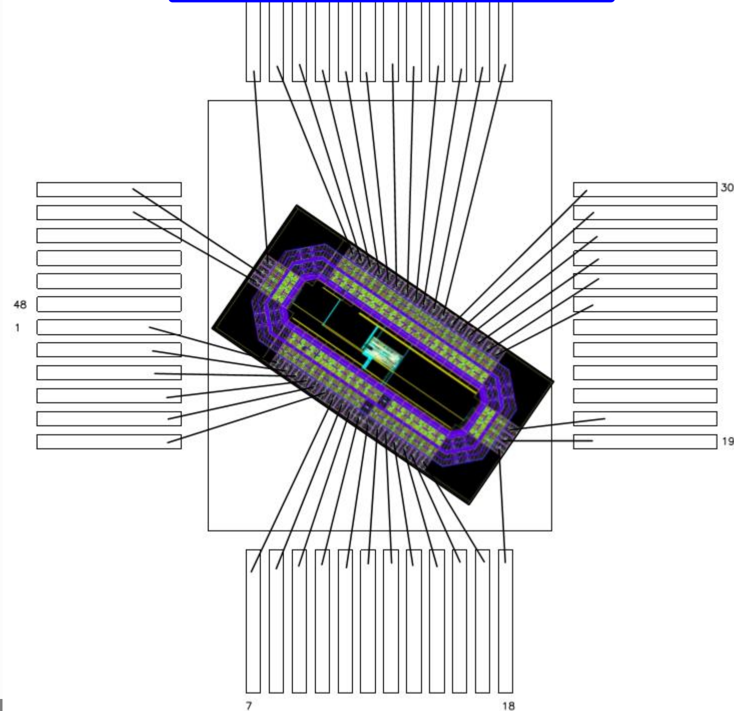
- Photo of layout
- Schematic of packages
- Bonding Diagram

Deliver the bonding diagram to foundries!

Chip on package



Chip on board



Packaging (Technical files)

- Photo of layout
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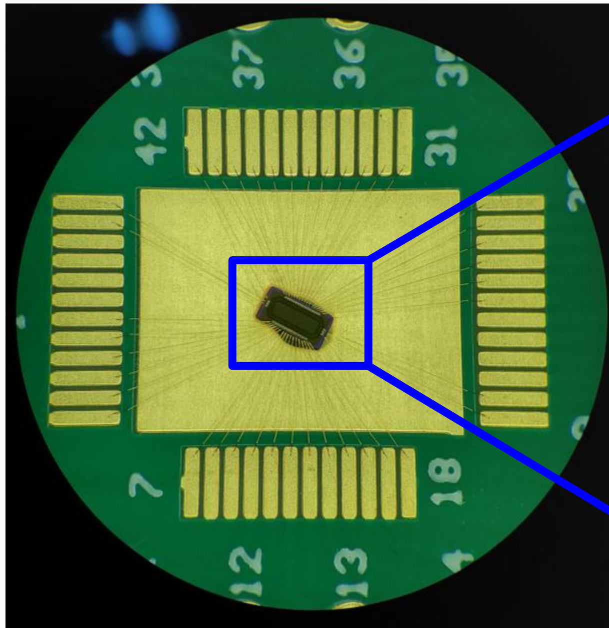
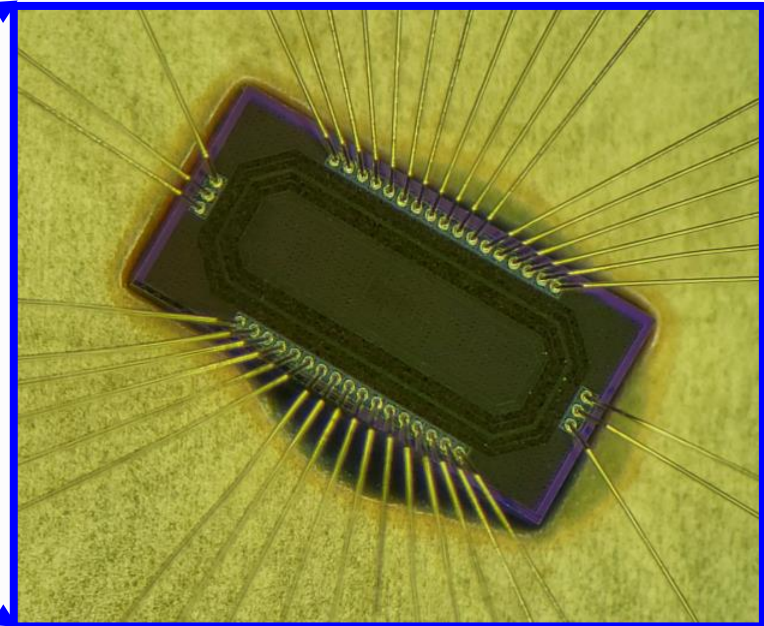
Deliver the bonding diagram to foundries!

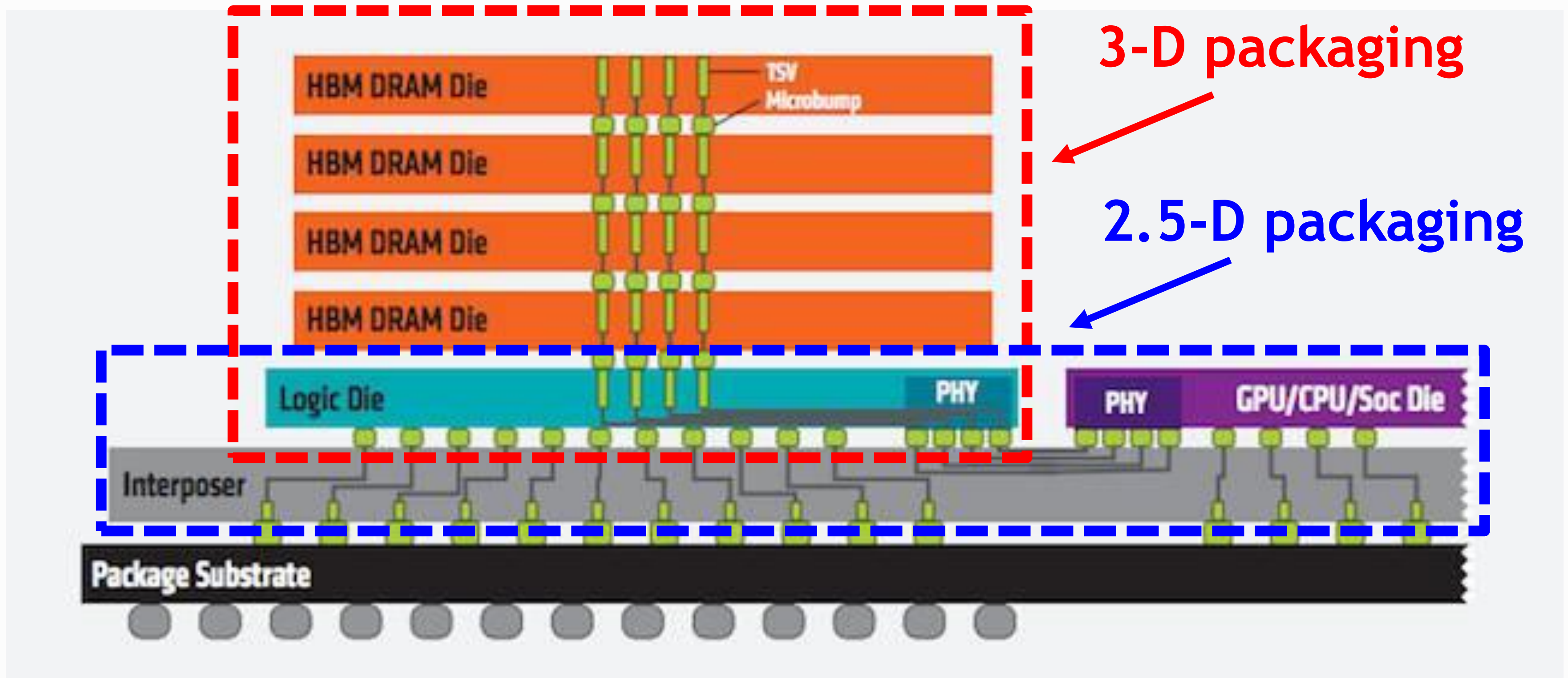




Remember the direction marks!!!

Advanced packaging

- 2.5-D: packaging, Silicon interposer (硅中介)
- 3-D: Stack packaging (层叠封装), TSV



Summary

- Two Important Rules Towards a Chip
  - Antenna, off-grid
- ESD Protection & PAD
  - ESD Introduction (Cause+Model+Influence)
  - ESD Protection (Concept+Architecture+Circuits)
- Floorplan
  - Pin-driven, Block-driven, Signal-driven
- Packaging
  - Introduction, Bonding

Reminder for next week

- Homework #1
  - Due on May 7th (Expired)
- Homework #2
  - Due on May 21th
- Project #1
  - Due on June 14th (with a short presentation)
  - Two project proposals (ADC & Two-stage opam)
  - Will have a short presentation