模拟集成电路课程设计（版图）
Layout in Analog Integrated Circuits

Assist. Prof. Jian Zhao
Prof. Guoxing Wang

Shanghai Jiao Tong University
School of Microelectronics
zhaojianycc@sjtu.edu.cn

Instructors

- **Time**
  - Lecture: Tuesday 14:00 to 15:00
  - Lab: Tuesday 15:00~17:30, Friday 14:00~17:30
- **Lecturer**
  - Assist. Prof. Jian Zhao (赵健) & Prof. Guoxing Wang
  - School of Microelectronics, Room 427
  - zhaojianycc@sjtu.edu.cn
- **Teaching Assistant**
  - Dr. Luo Jing (罗京)
  - School of Microelectronics, Room 404.
  - luojing@sjtu.edu.cn

Syllabus (New)

L1: Introduction

L2: Process, Active & Passive Components

L3: Process variation & Matching Issues

L4: Parasitic Effects

L5: ESD & Pads

L6: Floor planning & Package

L7: Design for Manufacture (Prof. Li Yongfu)

L8: Tracy (Advanced EDA tools by cadence)

L9: Project Review

Review of Lecture #3

- Source of Variations
- Corner Analysis
- Random Var., Mismatch & Monte-carlo
- Deterministic Mismatch
  - Intrinsic & Extrinsic Mismatch
  - Matching for MOSFET (Current & Voltage)
  - Matching for Resistor & Capacitor

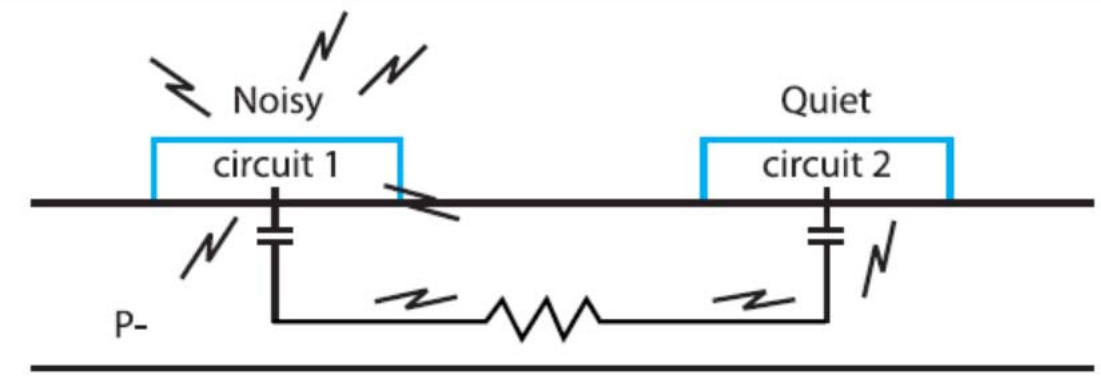
Outline of Lecture #4

- Parasitic effect (寄生效应) in IC design
- Parasitic capacitor & crosstalk (串扰)
  - Noise Crosstalk between interconnects
  - Parasitic capacitor with Noise & Stability
- Parasitic resistor & grounding issue (接地问题)
  - Grounding (single-point, multi-point)
- Parasitic BJT (Latch-up 闩锁效应) & protection
  - Parasitic BJT & Latch-up techniques
  - Guard ring technique and Examples
- Utilize Parasitic effects

Parasitic Effects in CMOS

- Parasitic Effects exist in Everywhere
  - CMOS transistor
  - Interconnects
  - Passive devices
  - Pads

Parasitic = unwanted!!!

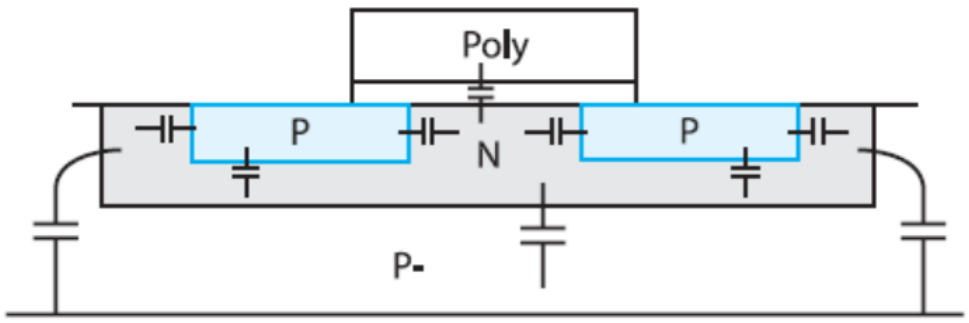


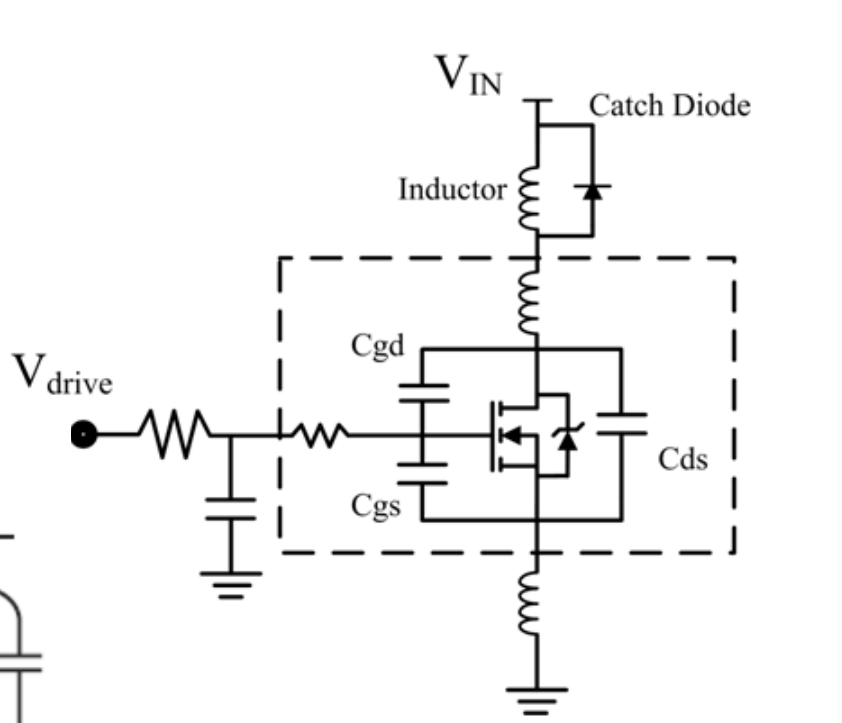
Metal	M1	M2	M3	M4
Min. Width	0.8	0.8	2.4	6.5
Cap/Unit Area (fF/μm^2)	5	3	2.5	1.5

Parasitic Effects in CMOS

- Parasitic effects deteriorates the performance
  - Bandwidth
  - Accuracy

This lecture sill introduce more practical cases!



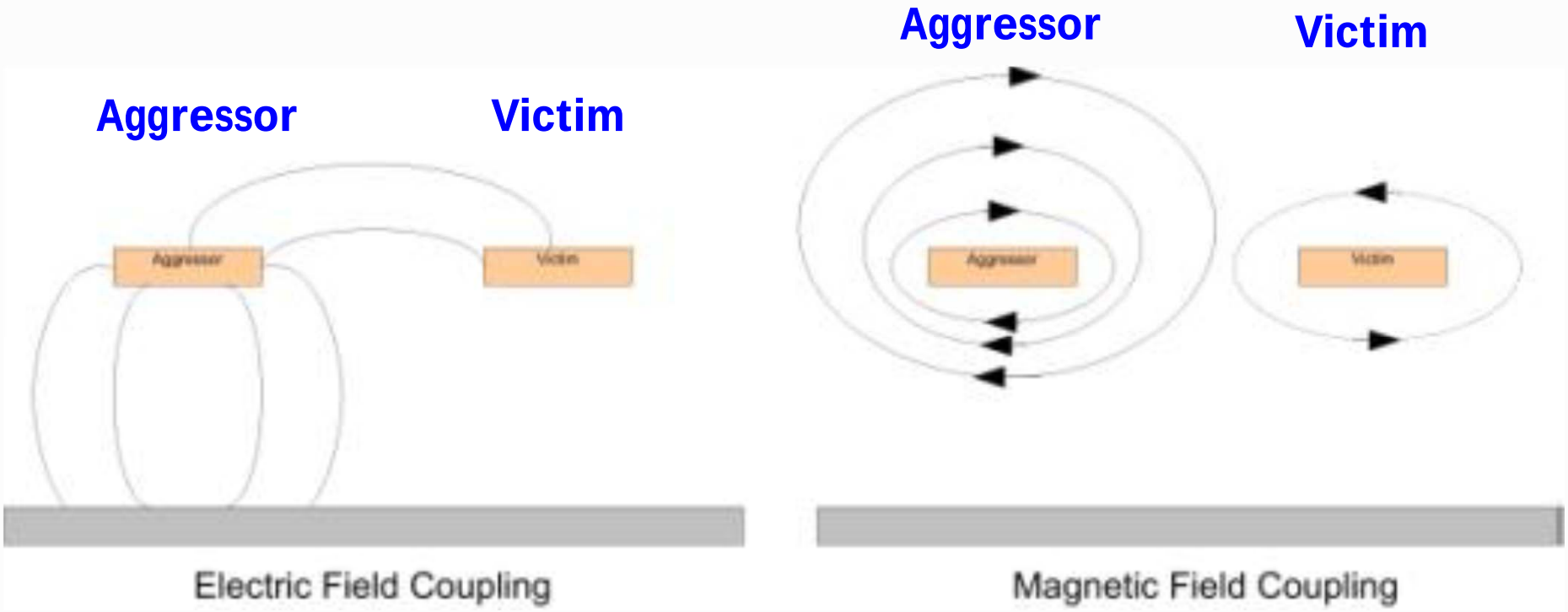


Outline of Lecture #4

- Parasitic effect in IC design
- Parasitic capacitor & crosstalk
  - Noise Crosstalk between interconnects
  - Parasitic capacitor with Noise & Stability
- Parasitic resistor & grounding issue
  - Grounding (single-point, multi-point)
- Parasitic BJT (Latch-up) protection
  - Parasitic BJT & Latch-up techniques
  - Guard ring technique and Examples
- Utilize Parasitic effects

Parasitic capacitor (Crosstalk, 串扰)

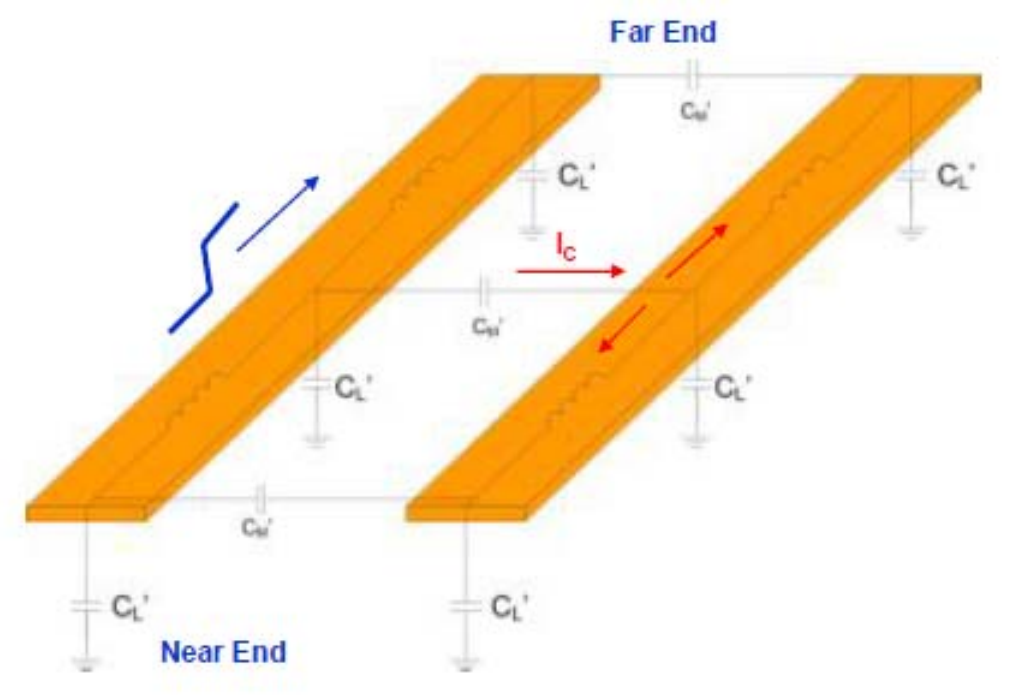
- Crosstalk between interconnects
  - Capacitive crosstalk
  - Inductive crosstalk



Parasitic capacitor (Crosstalk)

- Crosstalk between interconnects
  - Capacitive crosstalk (voltage-to-current)
  - Inductive crosstalk

$$I_C = C_M \frac{dV}{dt}$$

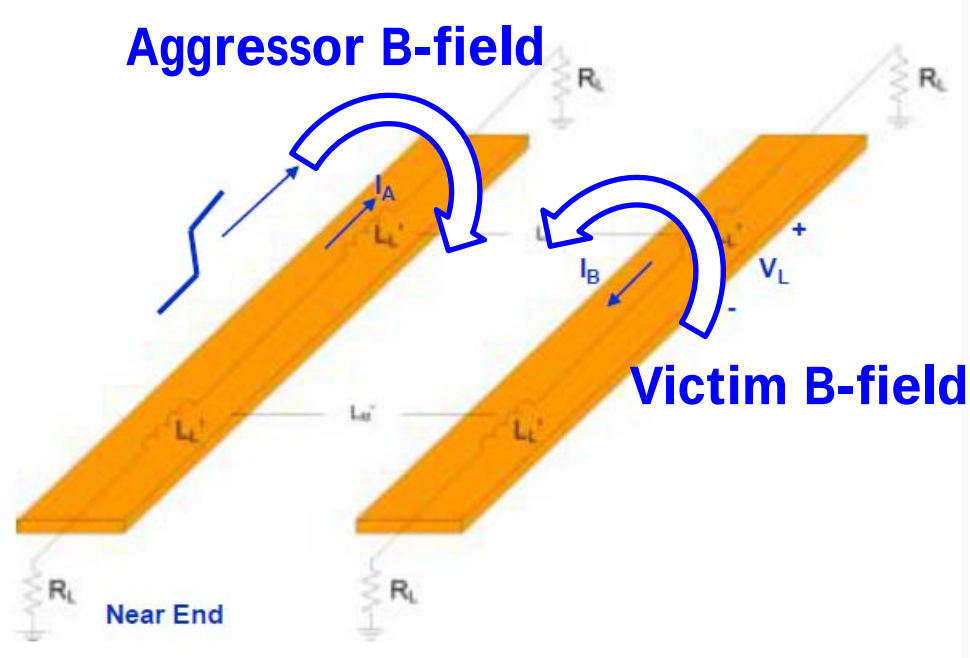


Parasitic inductor (Crosstalk)

- Noise Crosstalk between interconnects
  - Capacitive crosstalk
  - Inductive crosstalk (Current-to-current)

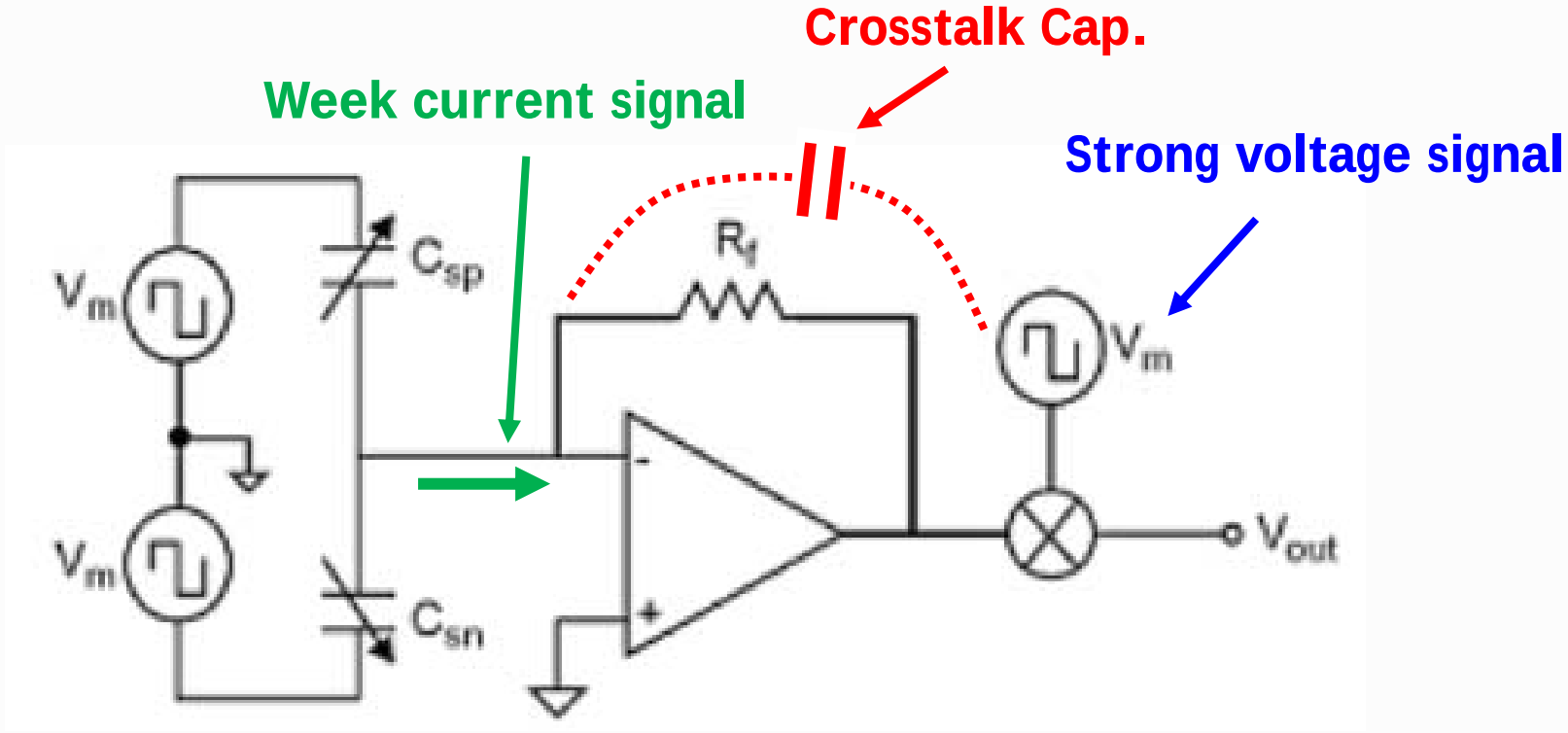
$$V_M = L_M \cdot \frac{dI_A}{dt}$$

$$V_L = L_L \cdot \frac{dI_B}{dt}$$



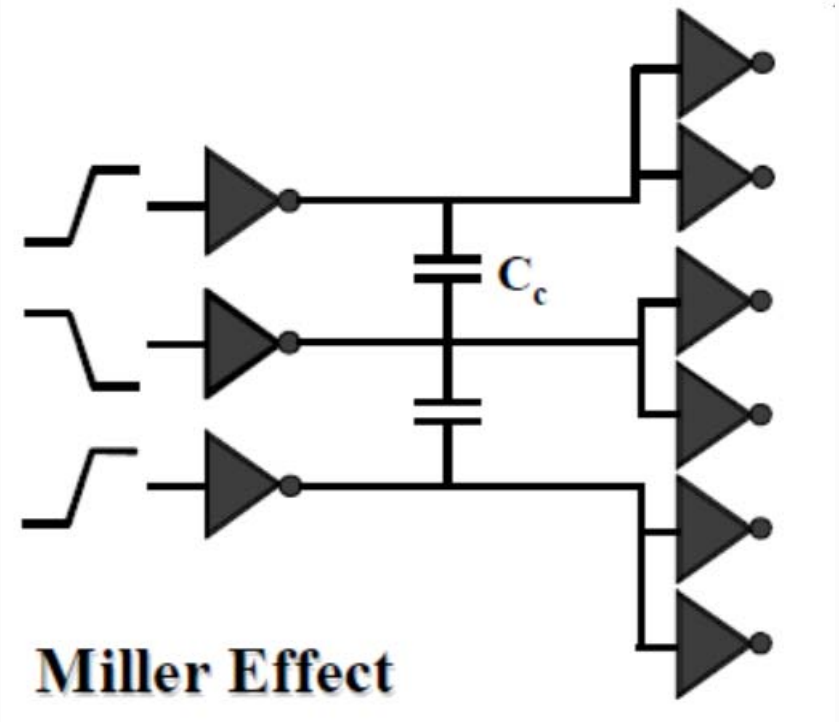
Parasitic capacitor (sensing error)

- Hazard of Capacitive crosstalk
  - Capacitive crosstalk seriously damage the performance of MEMS Gyroscope (陀螺仪)
  - Especially the orthogonal crosstalk



Parasitic capacitor (digital delay)

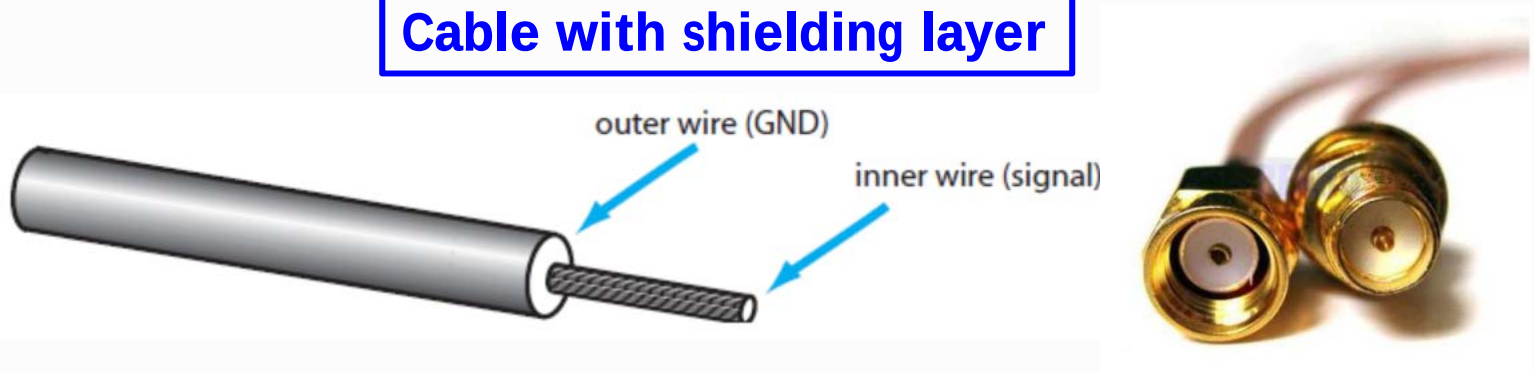
- Hazard of Capacitive crosstalk
  - Impact of neighboring signal activity on switching delay
  - When neighboring lines switch in opposite direction of victim line, delay increases



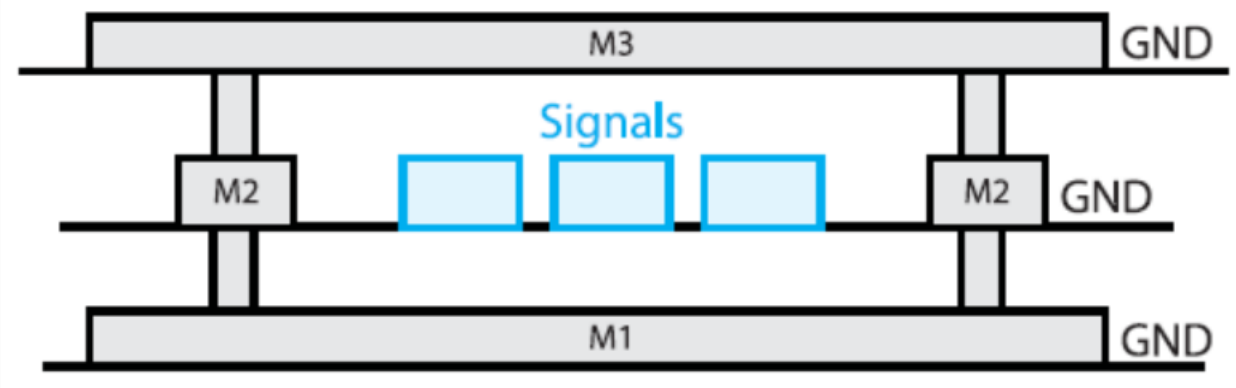
Parasitic capacitor (Crosstalk attenuation)

- Shielding (屏蔽) techniques
  - Significantly reduces the C_{para}

Cable with shielding layer

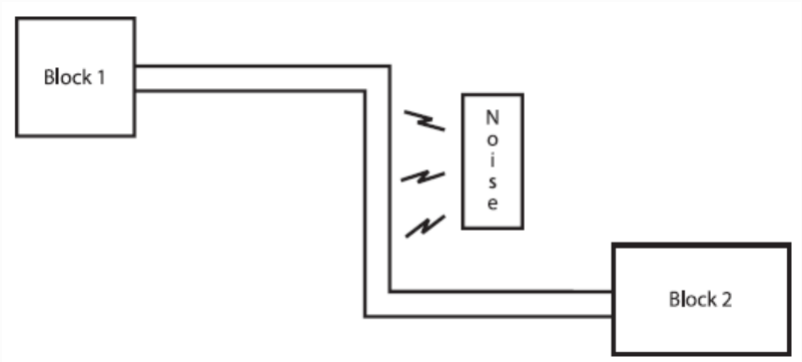


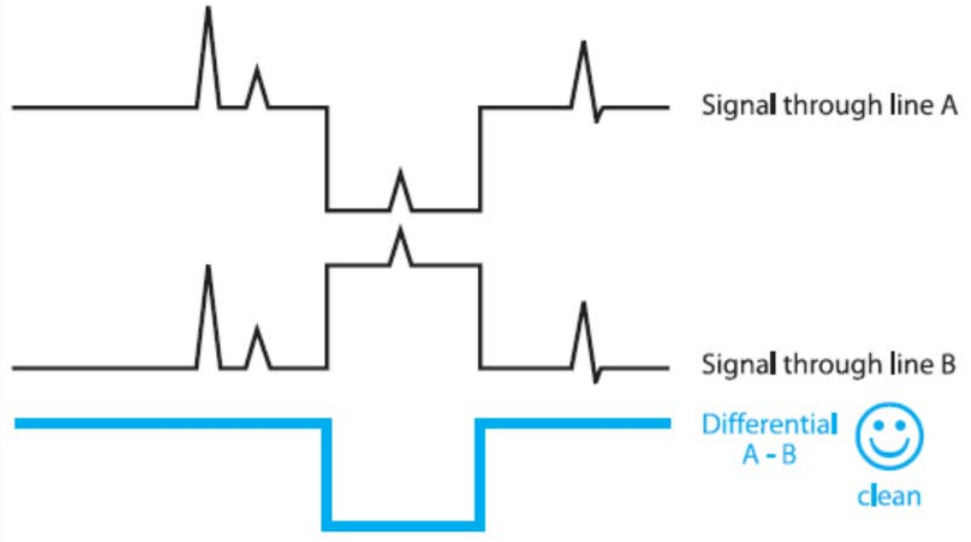
Cables with shielding layer (approaches in CMOS)



Parasitic capacitor (Crosstalk attenuation)

- Fully differential signal
  - Cancel the common-mode noise
  - The distance between two differential wire should be as close as possible



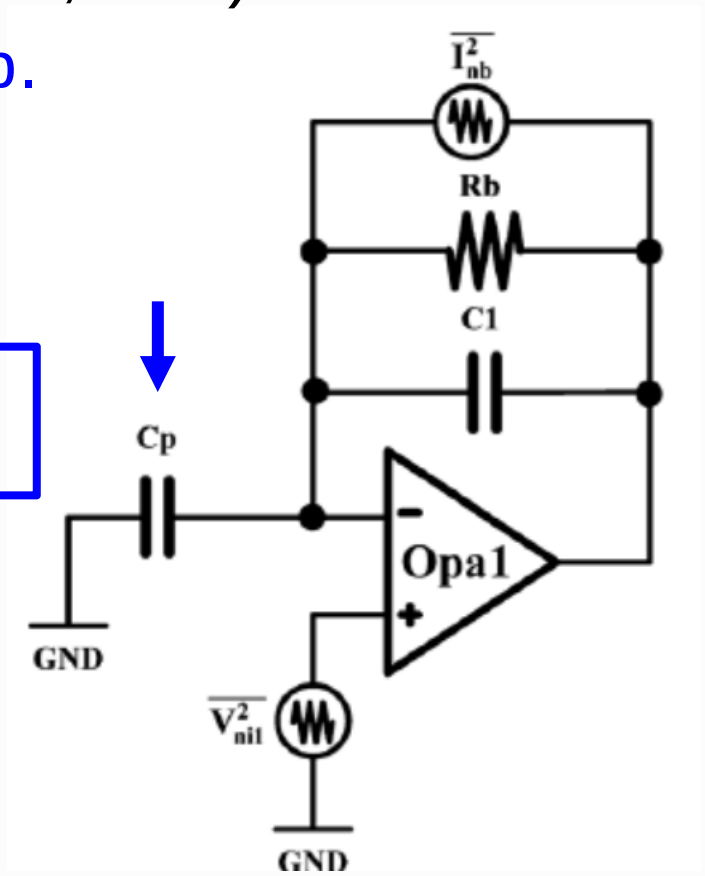


Parasitic capacitor (Noise)

- Parasitic capacitor with Noise
  - Input referred noise in TIA (in PPG, NIRS)
  - Gate Cap. + Pad Cap. + Wire Cap.

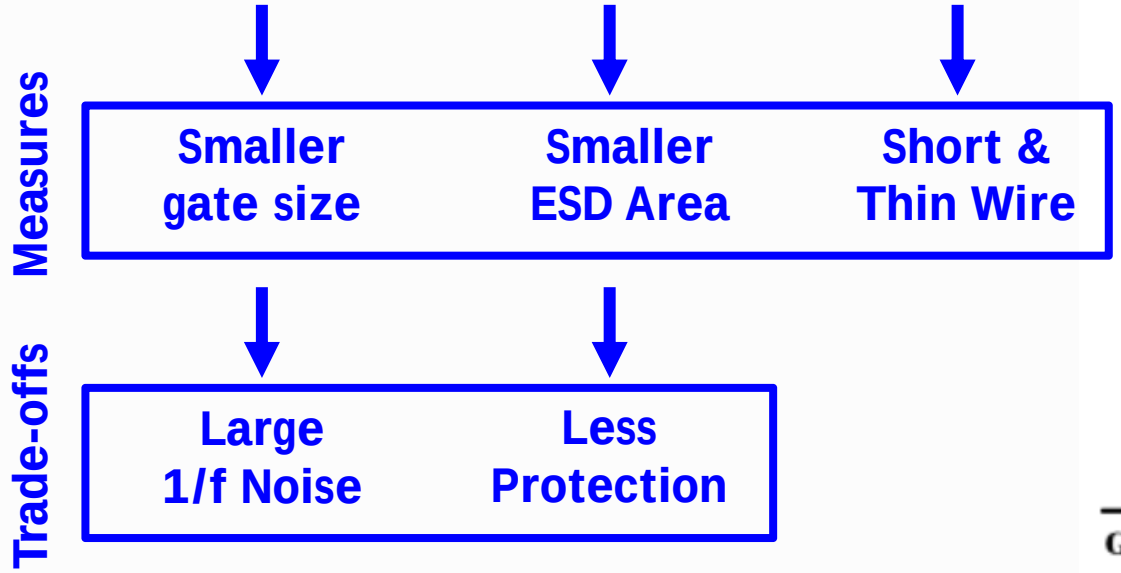
$$\overline{I_{ni}^2} = \overline{V_{ni1}^2}\left[\left(C_1 + C_p\right) s\right]^2 + \overline{I_{nb}^2}$$

Parasitic Capacitor C_p will deteriorates the input referred current noise!!!

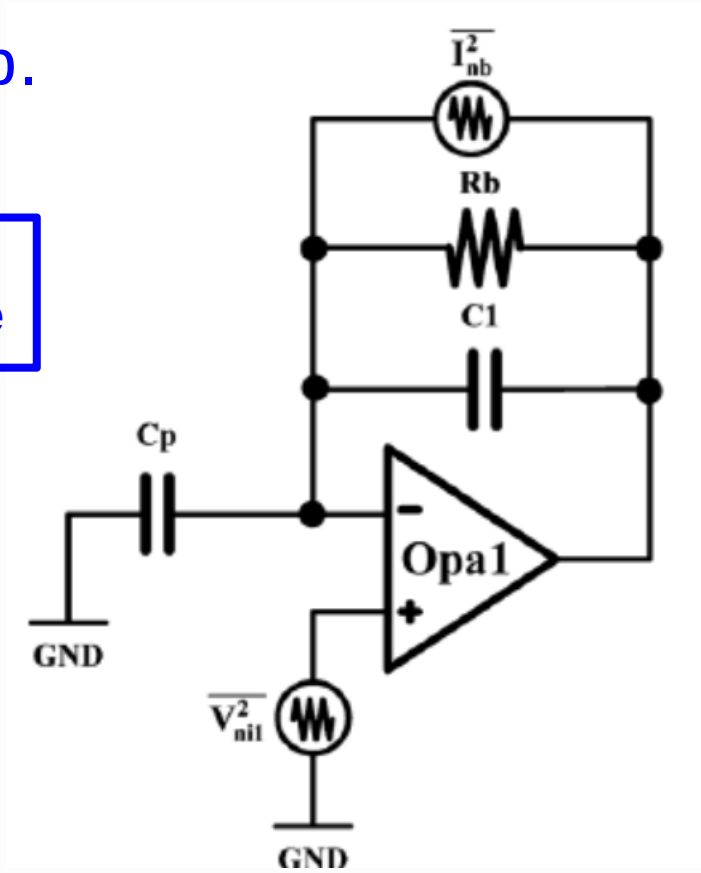


Parasitic capacitor (Noise & Trade-offs)

- Parasitic capacitor with Noise
  - Input referred noise in TIA
  - Gate Cap. + Pad Cap. + Wire Cap.

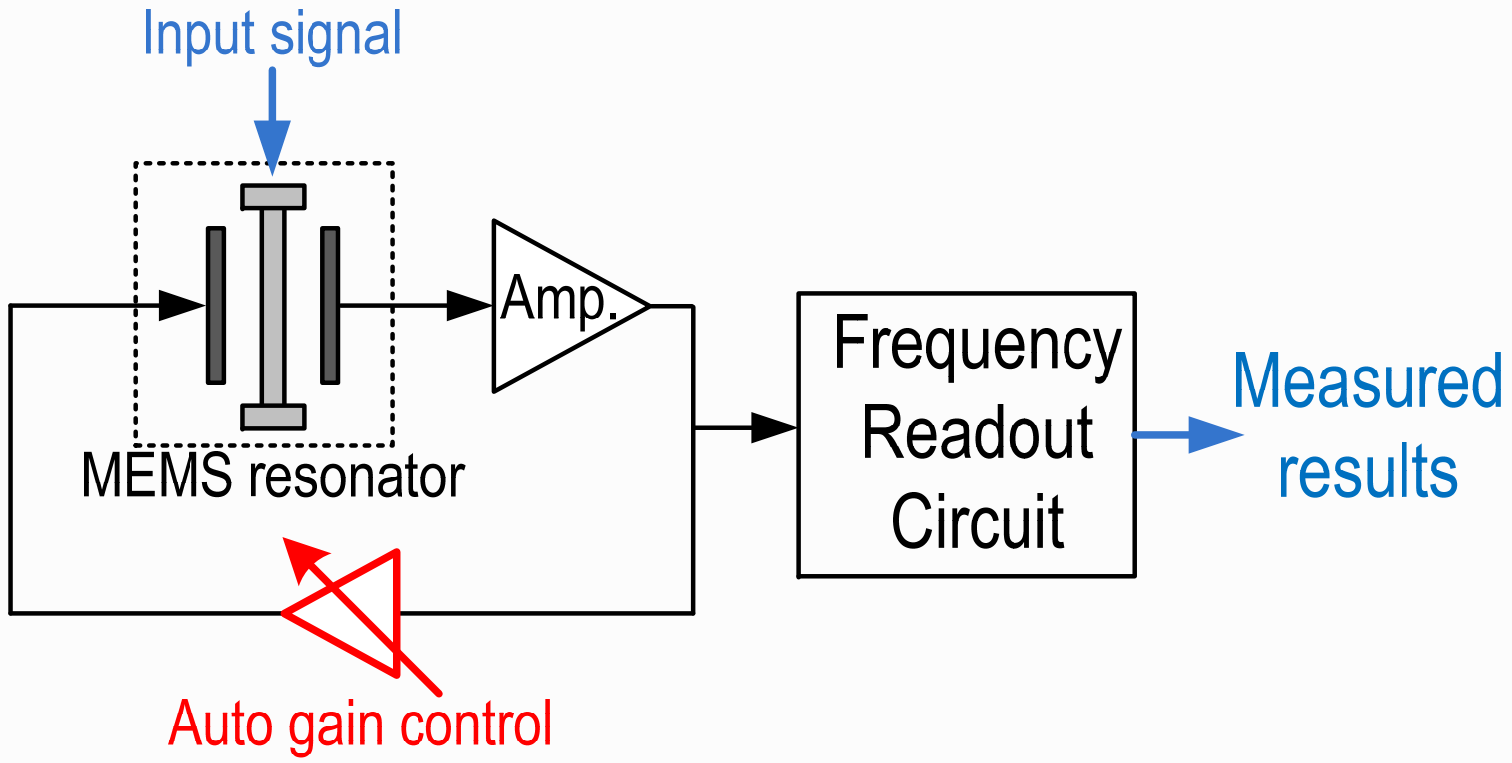


$$\overline{I_{ni}^2} = \overline{V_{ni1}^2}\left[(C_1 + C_p)\, s\right]^2 + \overline{I_{nb}^2}$$



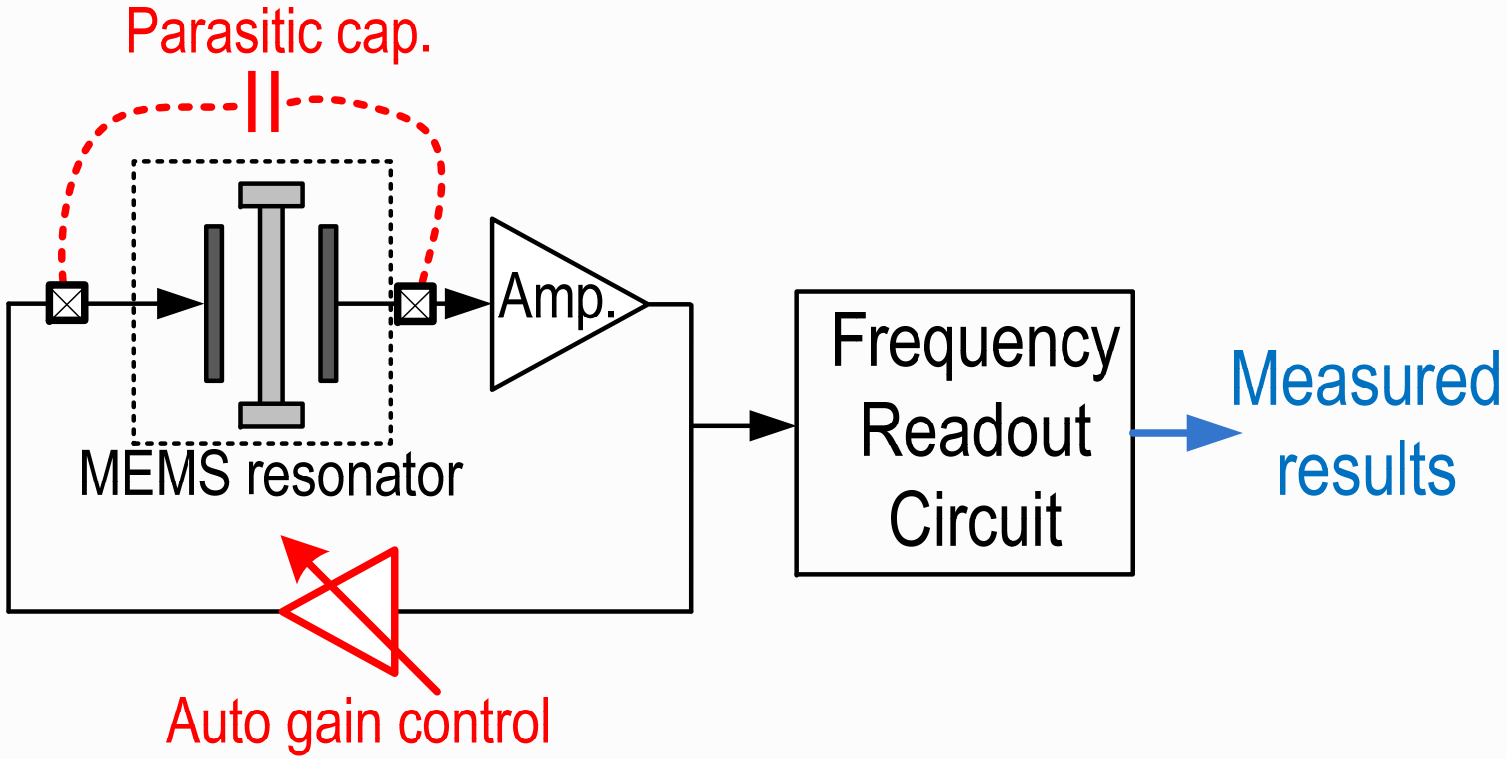
Parasitic capacitor (Stability)

- Parasitic capacitor with Stability
  - Background #1: Oscillator & AGC (Auto gain control)
  - Crosstalk forms a new path with higher gain & 360° phase shift



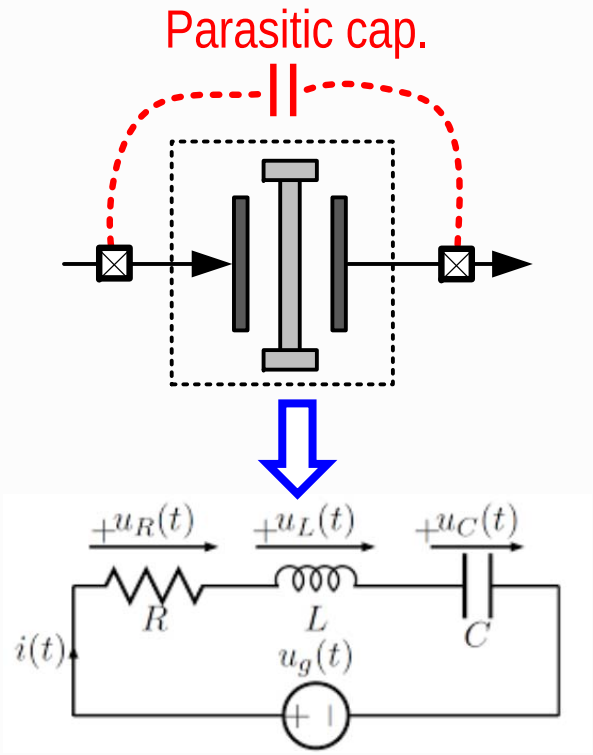
Parasitic capacitor (Stability)

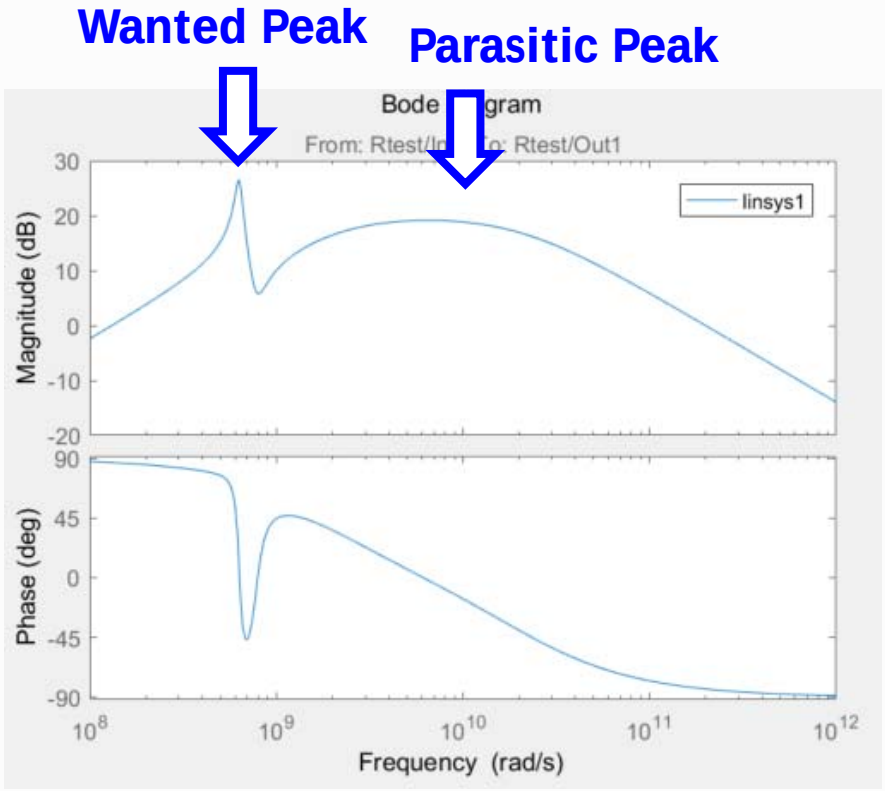
- Parasitic capacitor with Stability
  - Background #1: Oscillator & AGC (Auto gain control)
  - Crosstalk forms a new path with higher gain & 360° phase shift



Parasitic capacitor (Stability)

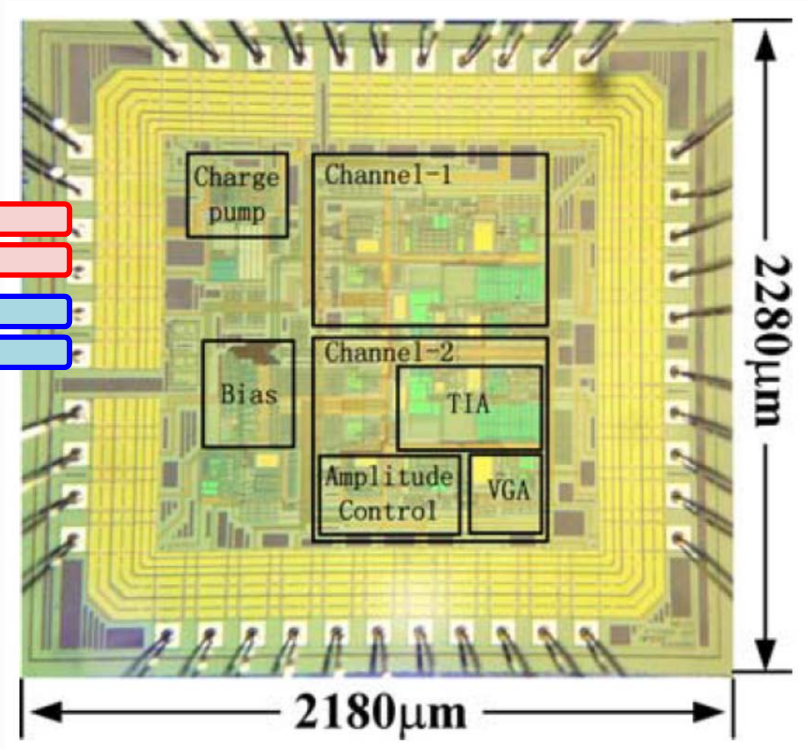
- Parasitic capacitor with Stability
  - Background #1: Oscillator & AGC (Auto gain control)
  - Crosstalk forms a new path with higher gain & 360° phase shift



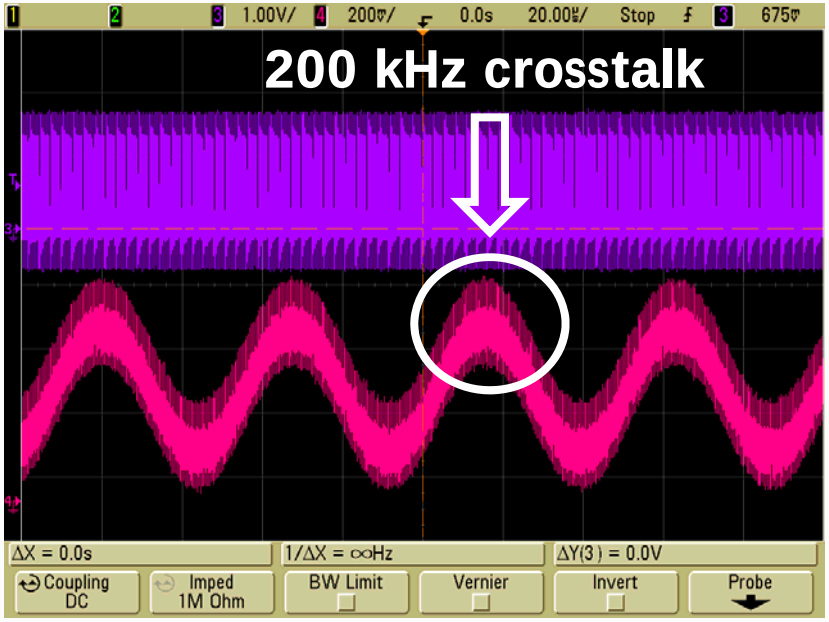


Parasitic capacitor (Stability)

- Parasitic capacitor with Stability
  - MEMS Resonator Sensor is an oscillator
  - Parasitic capacitor may take over to oscillate and by pass the sensors

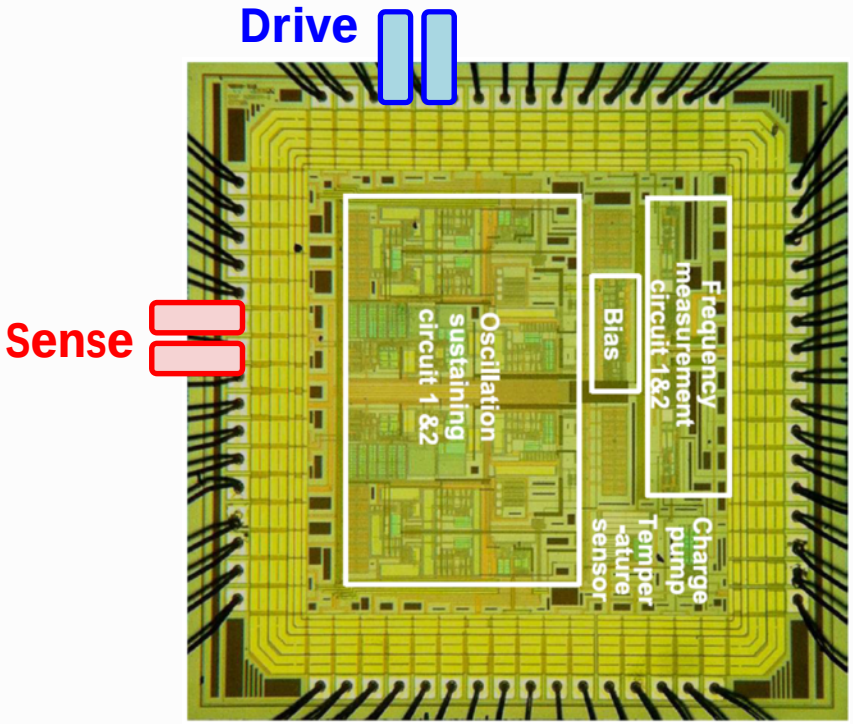


Insert a filter to verify the hypothesis!

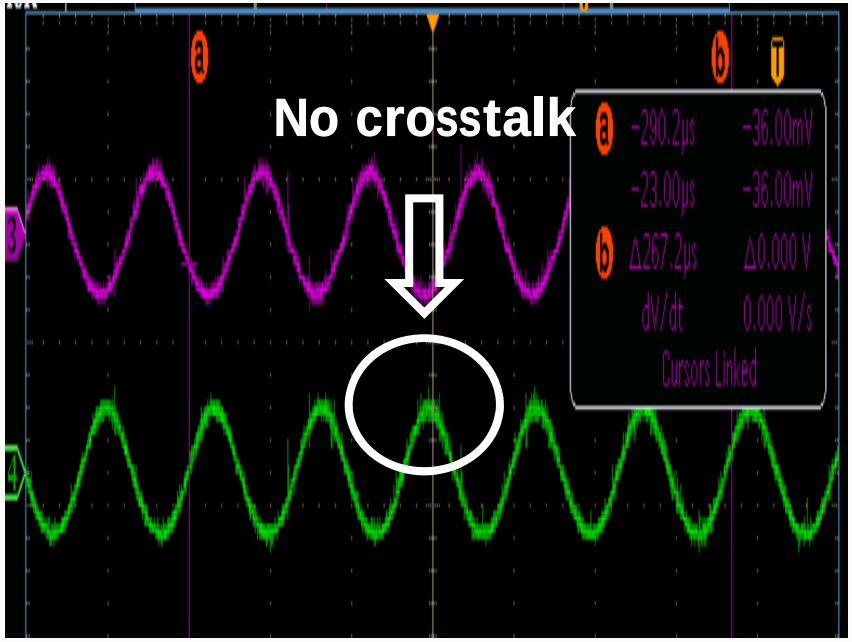


Parasitic capacitor (Stability)

- Parasitic capacitor with Stability
  - MEMS Resonator Sensor is an oscillator
  - Parasitic capacitor may take over to oscillate and by pass the sensors



Separate drive&sense port to eliminate the crosstalk!

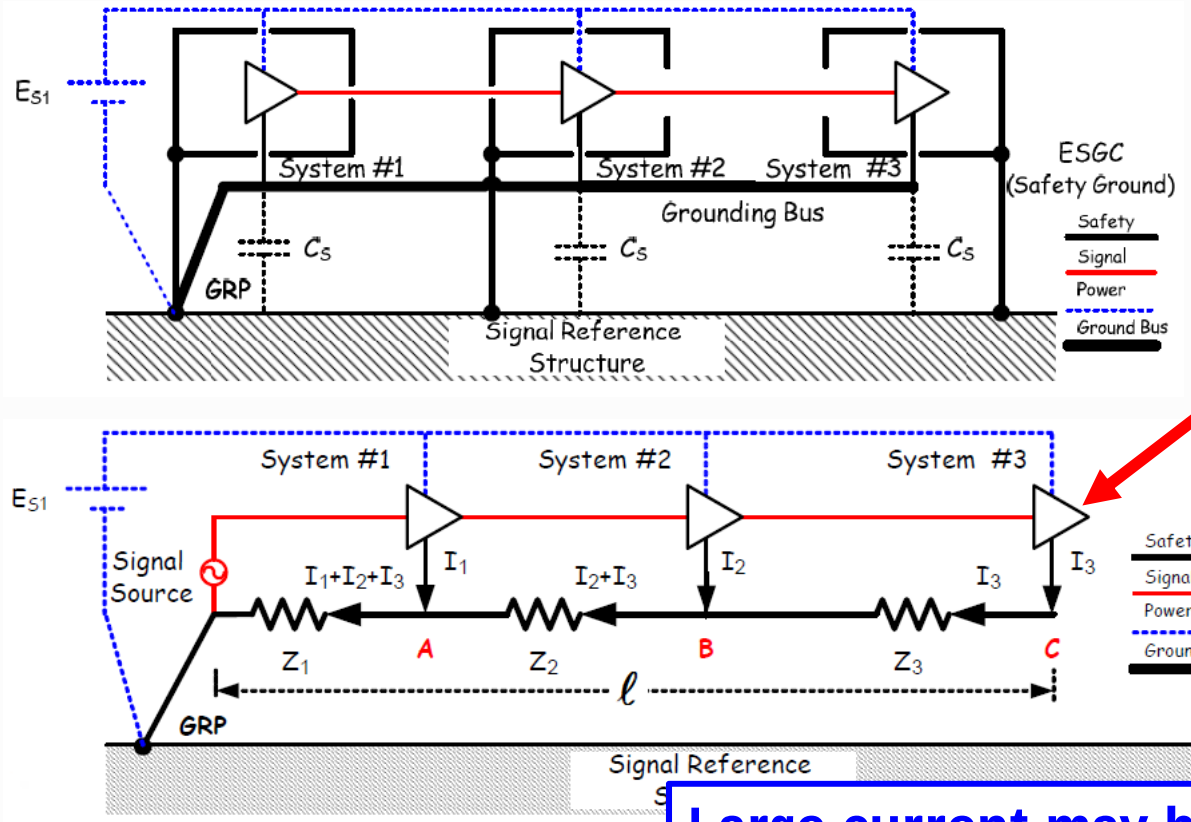


Outline of Lecture #4

- Parasitic effect in IC design
- Parasitic capacitor & crosstalk
  - Noise Crosstalk between interconnects
  - Parasitic capacitor with Noise & Stability
- Parasitic resistor & grounding issue
  - Grounding (single-point, multi-point)
- Parasitic BJT (Latch-up) protection
  - Parasitic BJT & Latch-up techniques
  - Guard ring technique and Examples
- Utilize Parasitic effects

Parasitic resistors (Grounding)

- Parasitic resistors and grounding ISSUE!
  - Ground coupling in “Daisy Chain” grounding topology

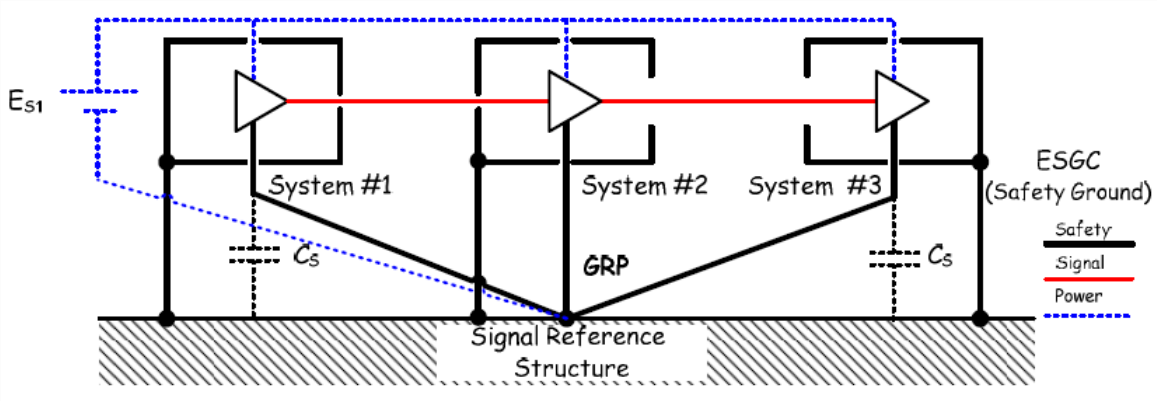


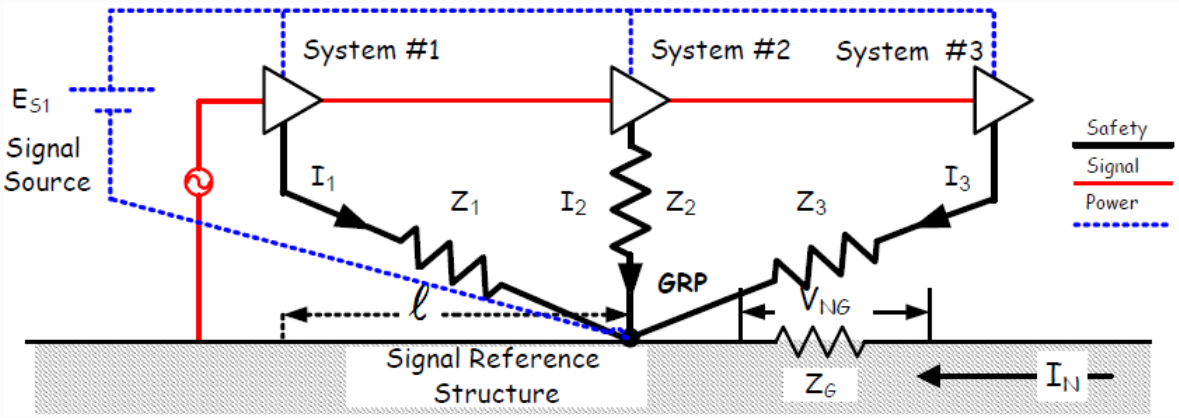
Things get even worse if I3 is large!!!

Large current may highlight the influence of parasitic resistance!!!

Parasitic resistance (Grounding)

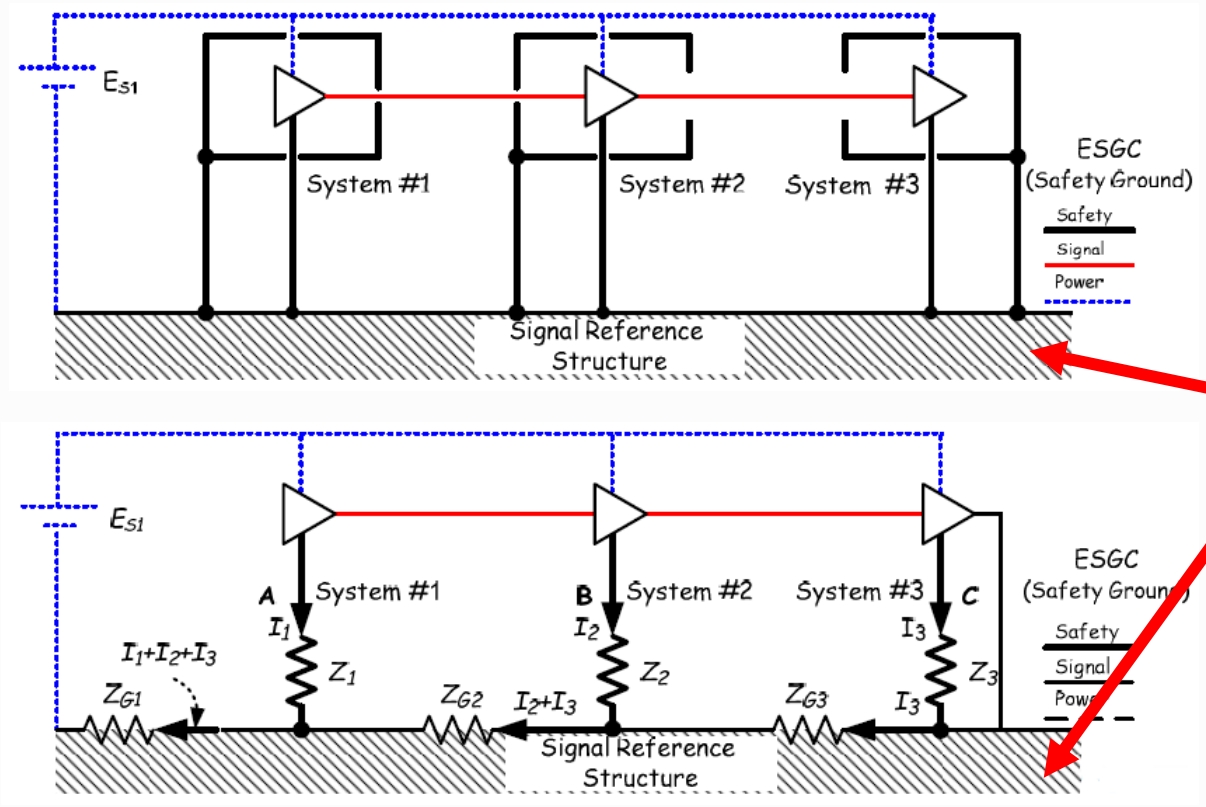
- Good way to ground the circuit blocks
  - "Star" single point grounding
  - Multi-point grounding





Parasitic resistance (Grounding)

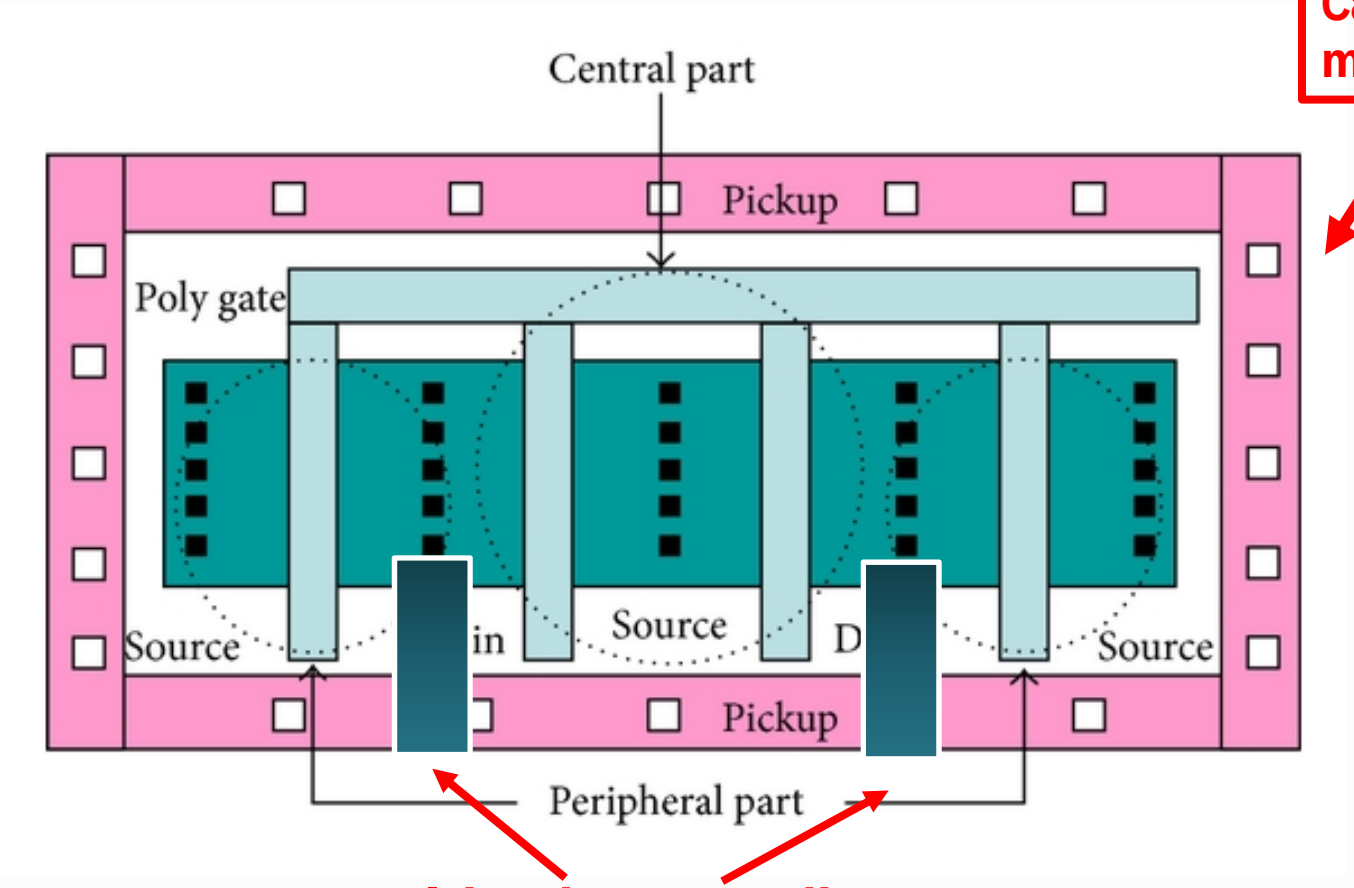
- Good way to ground the circuit blocks
  - "Star" single point grounding
  - Multi-point grounding



Can be large metal plane!

Parasitic resistance (Guard ring)

- Ground the circuit blocks by using guard ring
  - Guard ring is an adjacent Power/GND

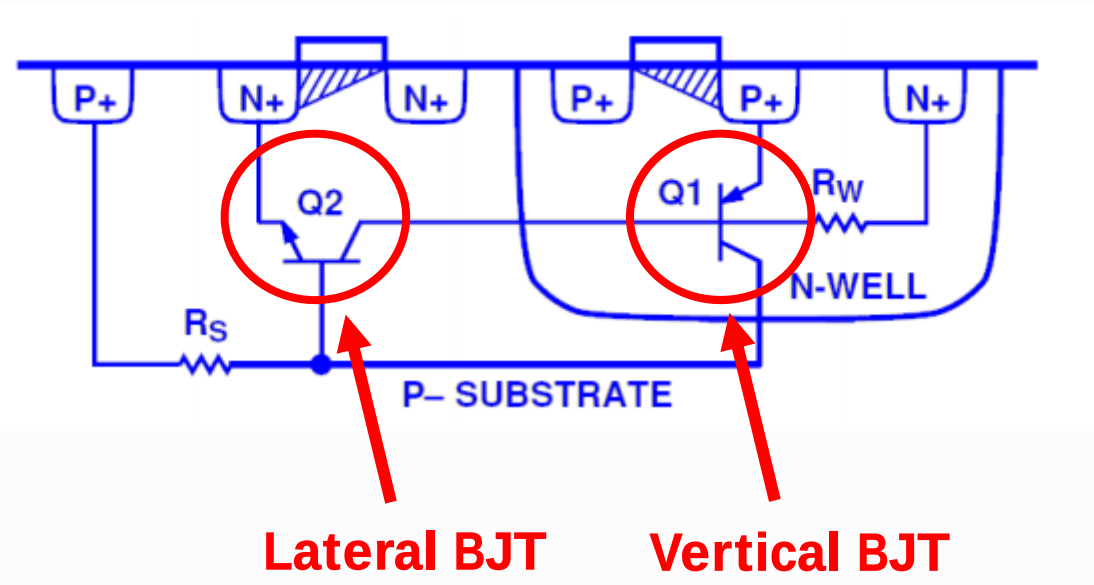


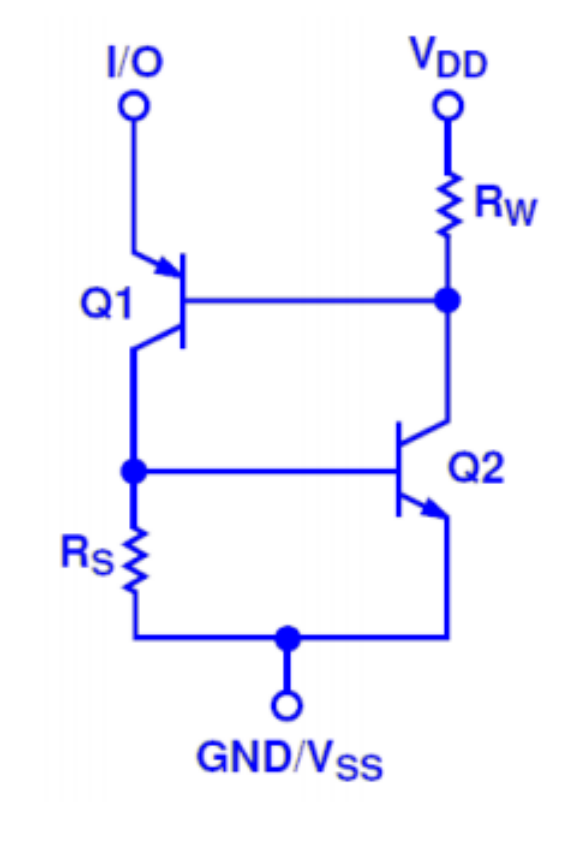
Outline of Lecture #4

- Parasitic effect in IC design
- Parasitic capacitor & crosstalk
  - Noise Crosstalk between interconnects
  - Parasitic capacitor with Noise & Stability
- Parasitic resistor & grounding issue
  - Grounding (single-point, multi-point)
- Parasitic BJT (Latch-up) protection
  - Parasitic BJT & Latch-up techniques
  - Guard ring technique and Examples
- Utilize Parasitic effects

Parasitic BJTs

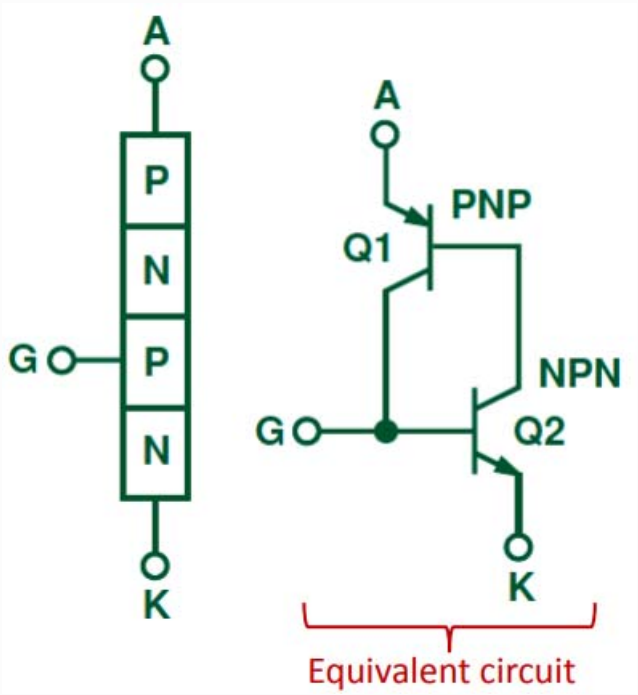
- Parasitic BJTs in CMOS
  - Two major BJTs are formed by the parasitic effects in CMOS process

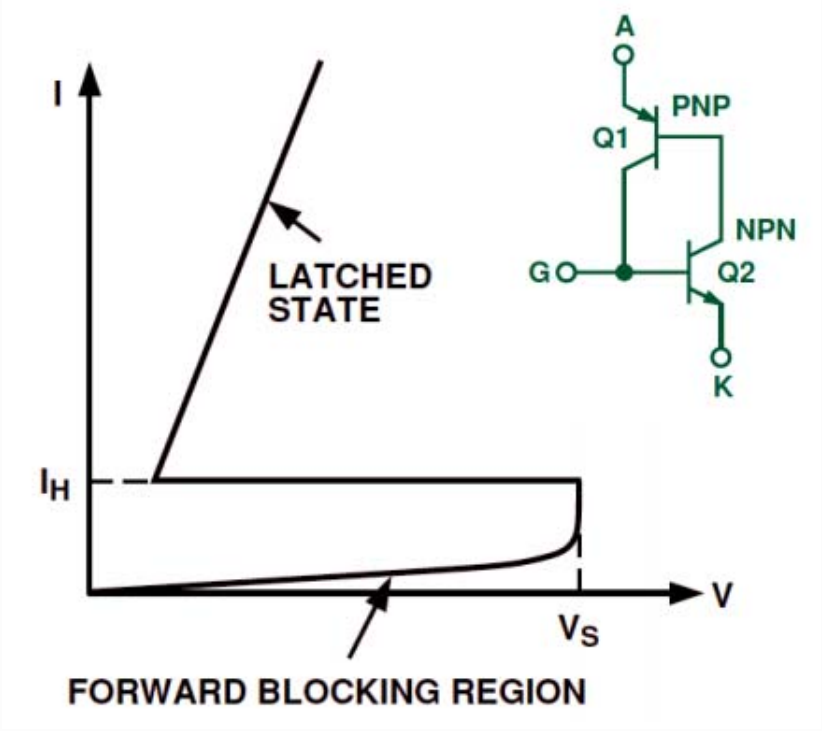




Parasitic BJTs

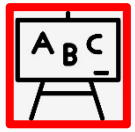
- Residual Silicon Controlled Rectifier (SCR, 可控硅)
  - The parasitic bipolar devices in a CMOS chip create a device known as SCR
  - Initially OFF, triggered by I_H or V_S, latched.



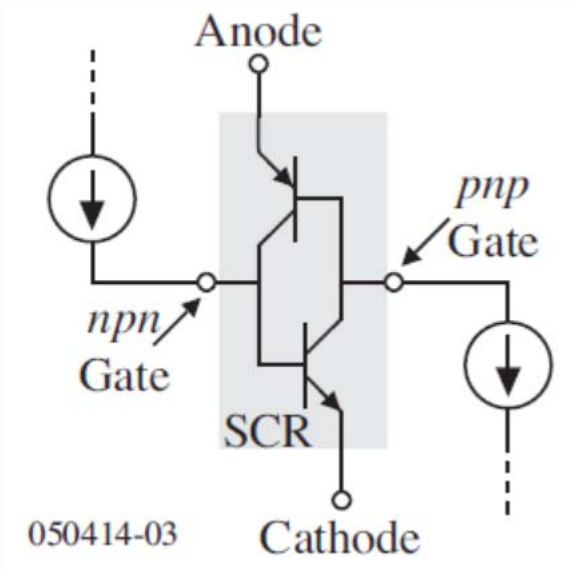


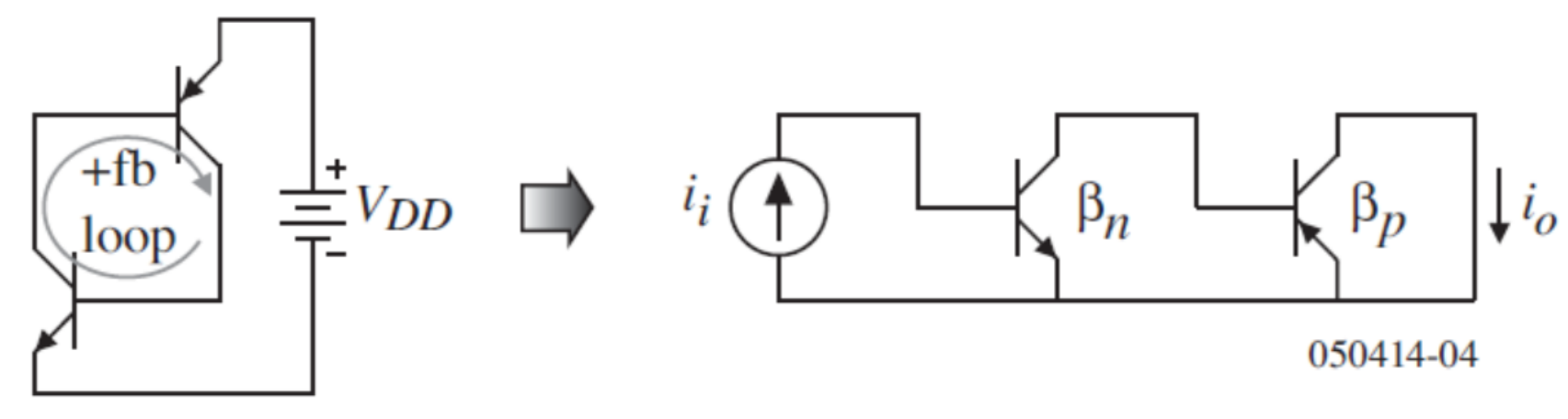
How to trigger the parasitic SCR

- Latch-up conditions
  - Beta_n * Beta_p >1
  - An injector
  - A stimulus



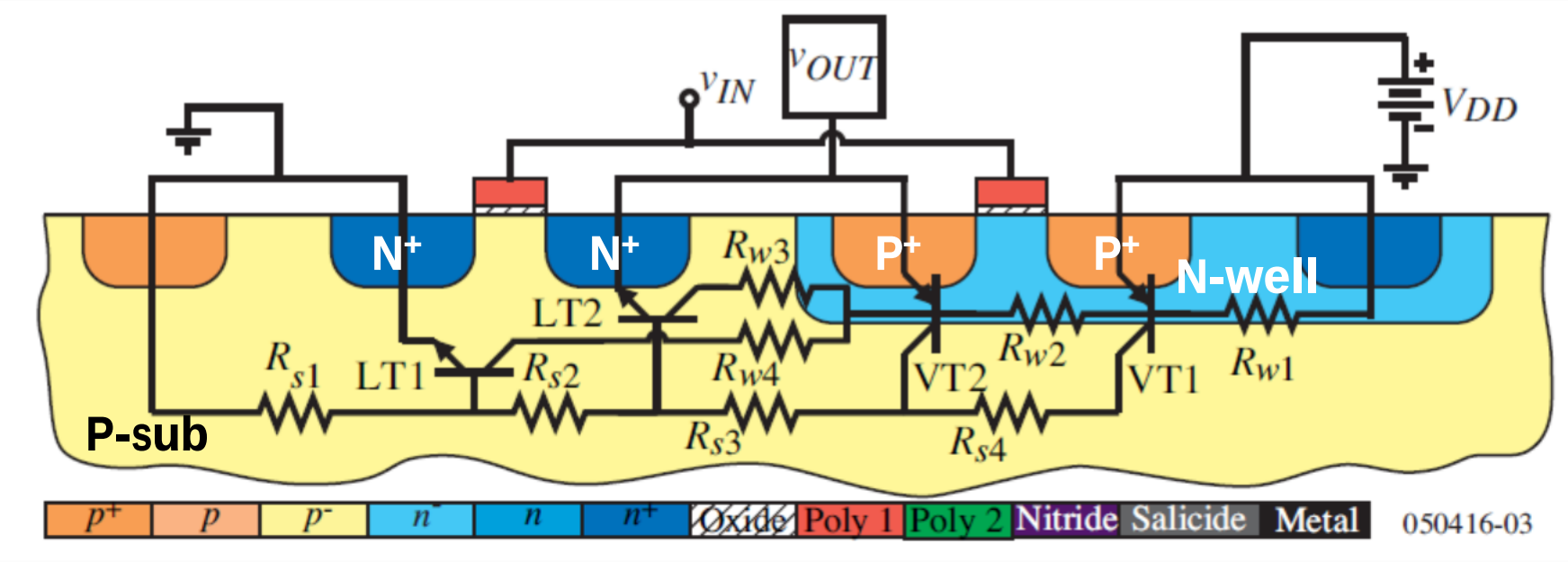
$$\frac{i_o}{i_i} \approx \beta_p \beta_n$$





Parasitic BJTs (Trigger)

- Latch-up triggering
  - LT2 and VT2 can trigger the latch-up



Parasitic components:

Lateral BJTs LT1 and LT2

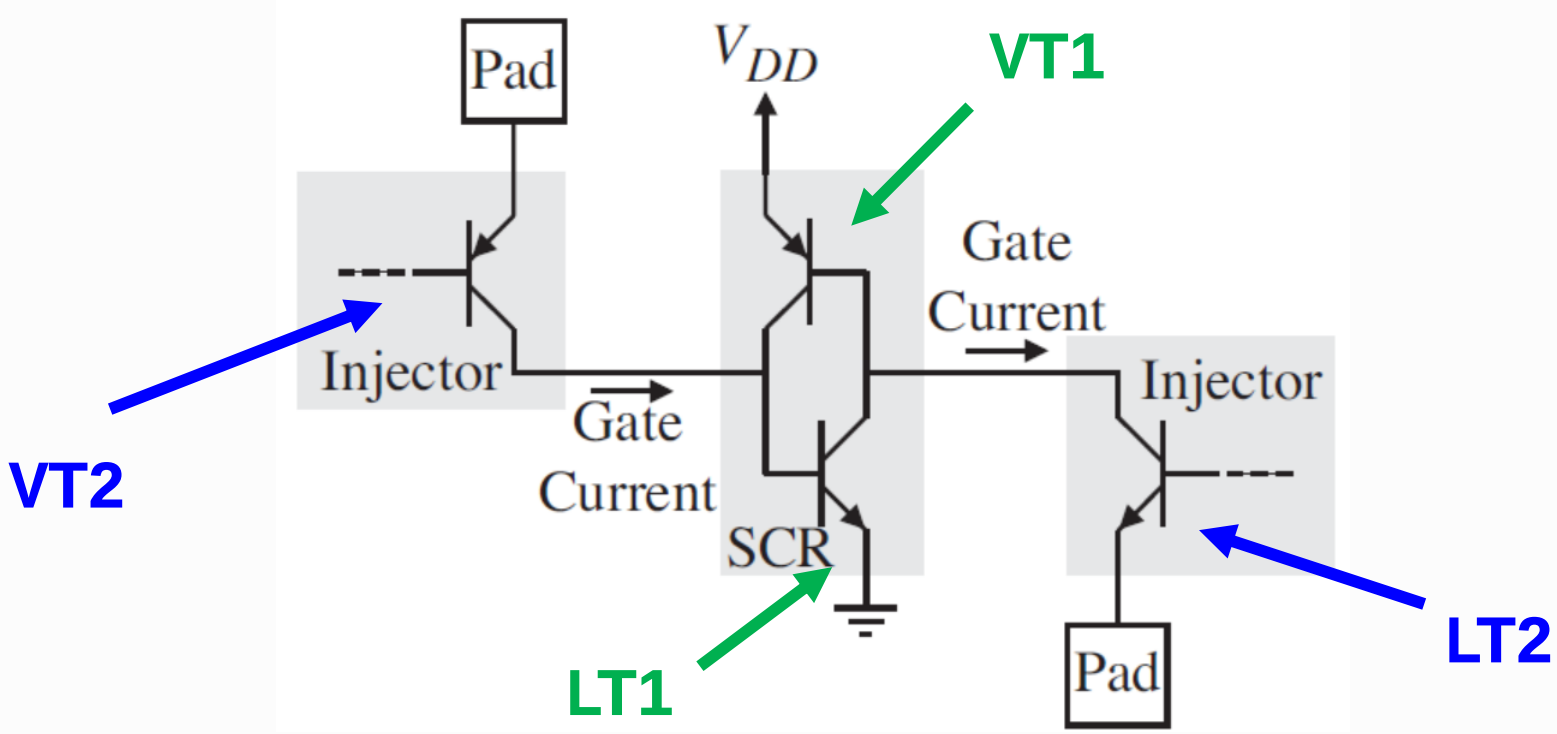
Vertical BJTs VT1 and VT2

Bulk substrate resistances R_{s1}, R_{s2}, R_{s3}, and R_{s4}

Bulk well resistances R_{w1}, R_{w2}, R_{w3}, and R_{w4}

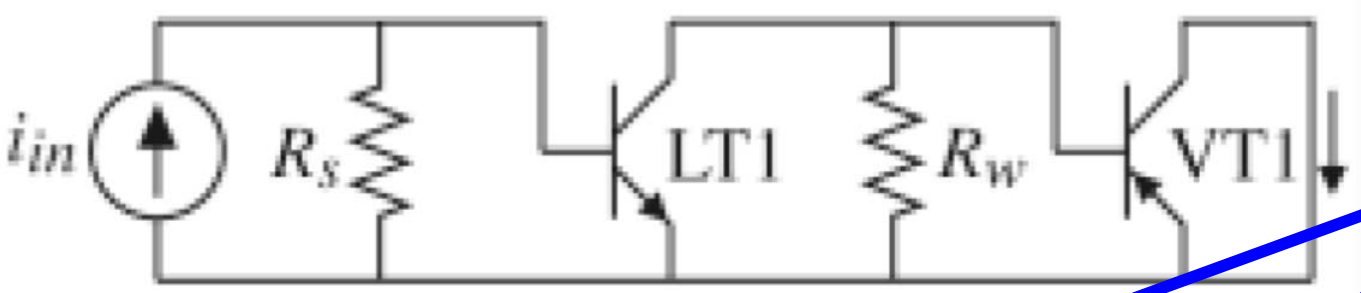
Parasitic BJTs (Trigger)

- Latch-up triggering
  - LT2 and VT2 can trigger the latch-up



Parasitic BJTs (Trigger)

- Latch-up attenuation
  - **Path isolation** or **Current shunting** can mitigate the latch-up issue



$$\frac{i_o}{i_i} \approx \beta_p \beta_n$$

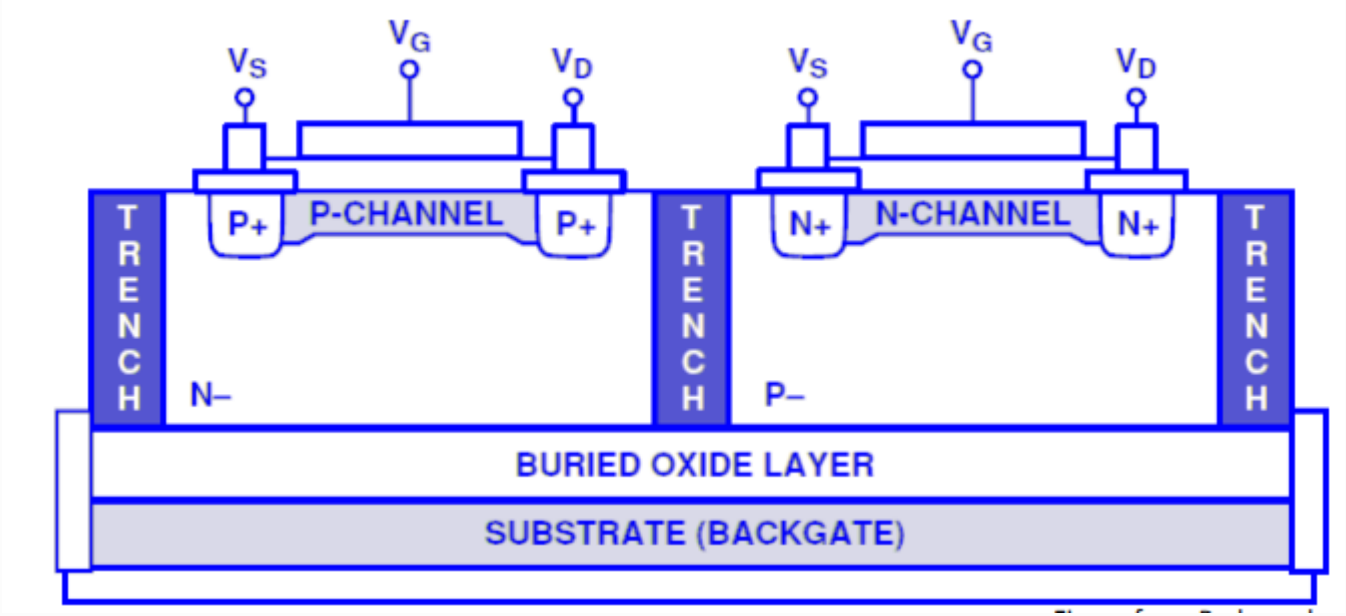
$$\frac{i_{out}}{i_{in}} = \beta_{P1}\left(\frac{R_W}{R_W + r_{\pi P1}}\right)\beta_{N1}\left(\frac{R_S}{R_S + r_{\pi N1}}\right)$$

$$= \beta_{P1}\beta_{N1}\left(\frac{R_W}{R_W + \frac{\beta_{P1}V_t}{I_{P1}}}\right)\left(\frac{R_S}{R_S + \frac{\beta_{N1}V_t}{I_{P2}}}\right)$$

Guard-ring technique

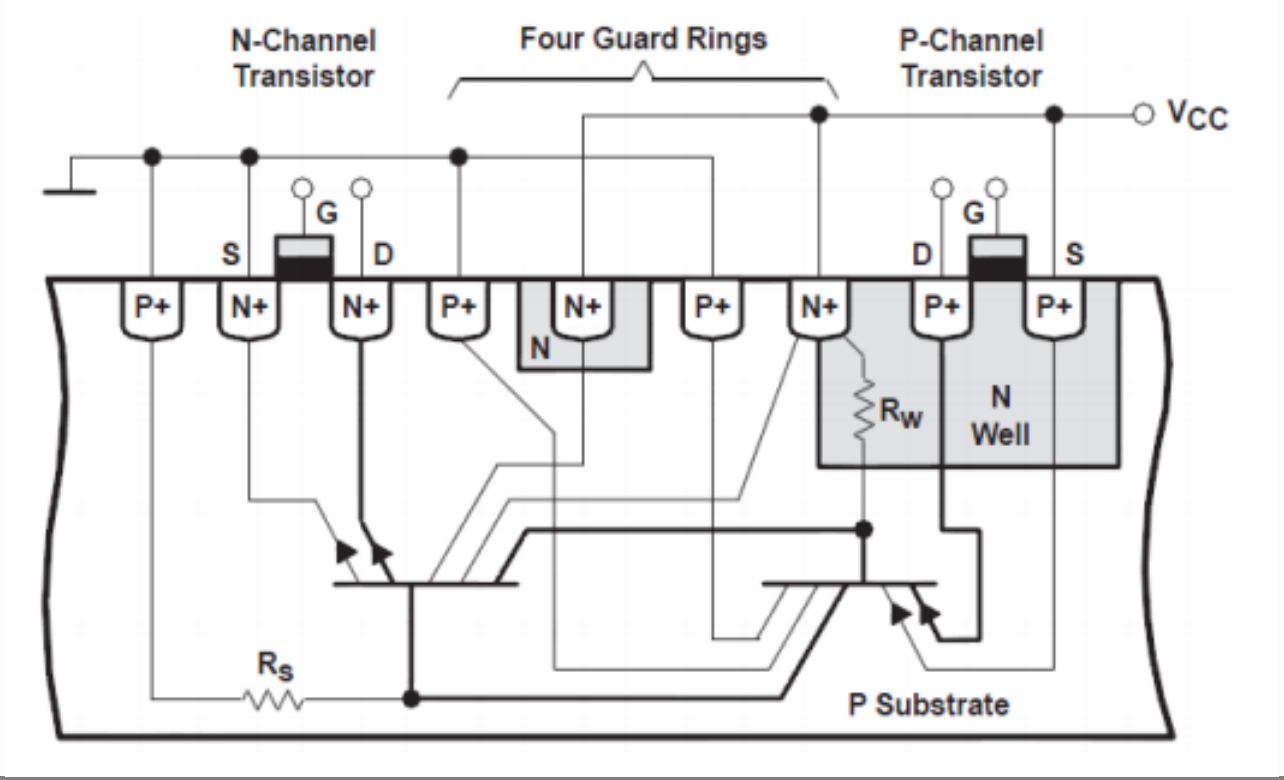
- Latch-up prevention
  - Stay below the absolute maximum ratings of the chip.
  - Isolate the NMOS and PMOS devices using an oxide trench together with a buried oxide layer

Extra-process required!!!



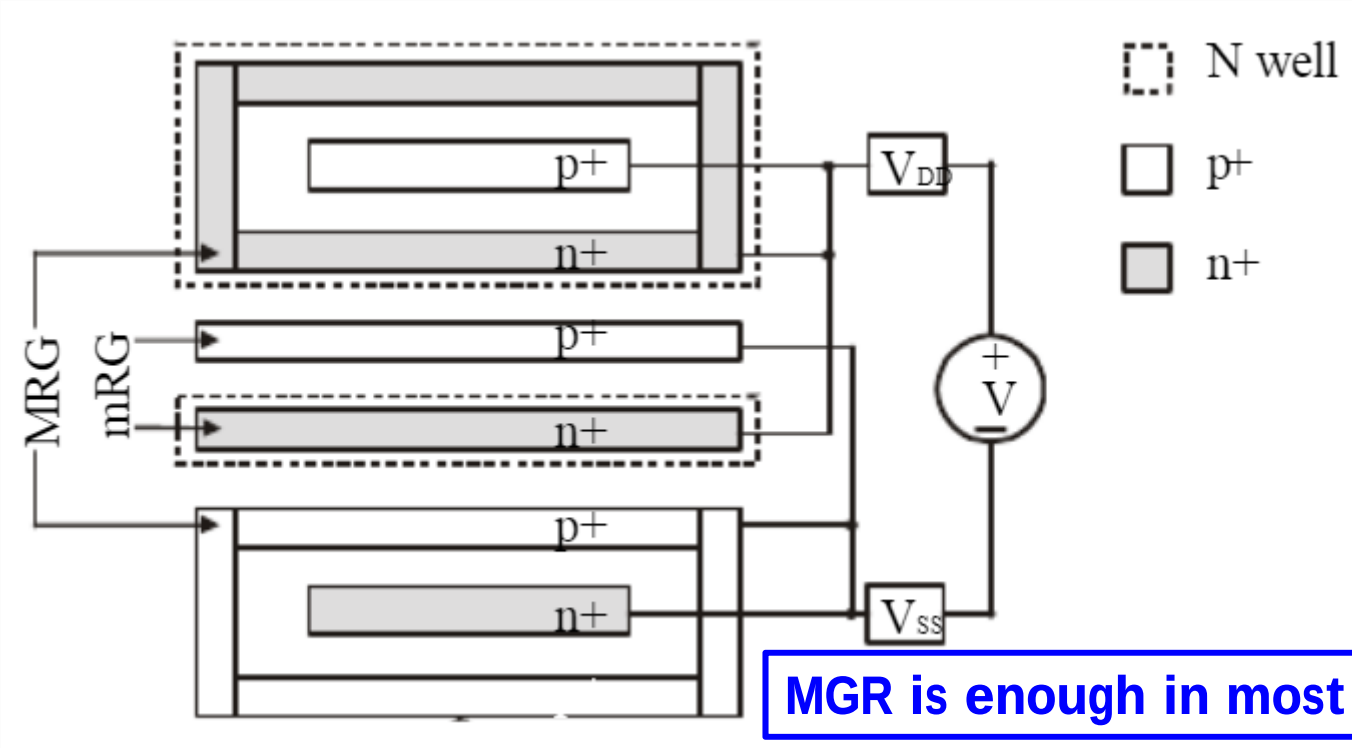
Guard ring examples

- Latch-up prevention
  - If you cannot include an oxide trench, then use guard rings around your devices
  - MGR (Majority carriers), mGR (minority carriers)



Guard ring examples

- Latch-up prevention
  - If you cannot include an oxide trench, then use guard rings around your devices
  - MGR (Majority carriers), mGR (minority carriers)



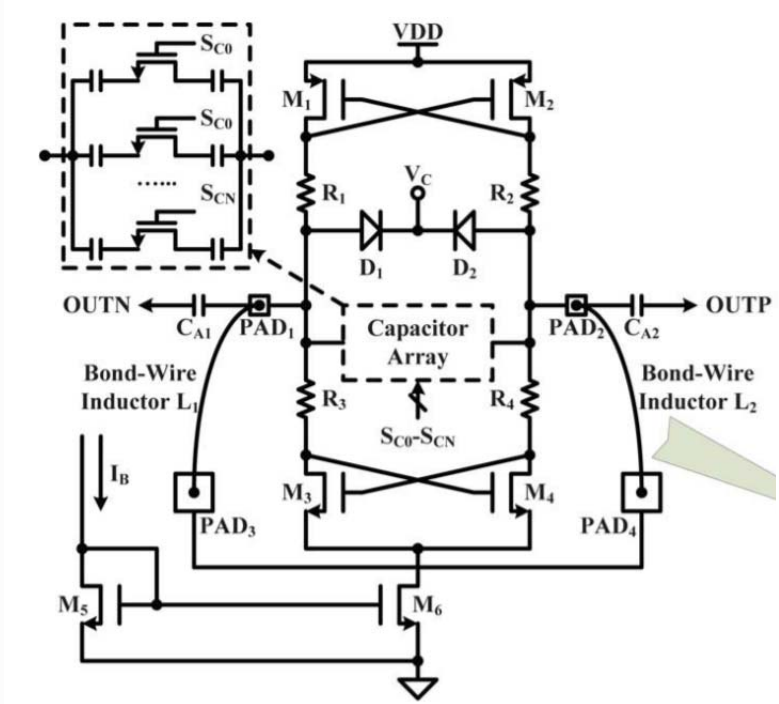
MGR is enough in most cases!!!

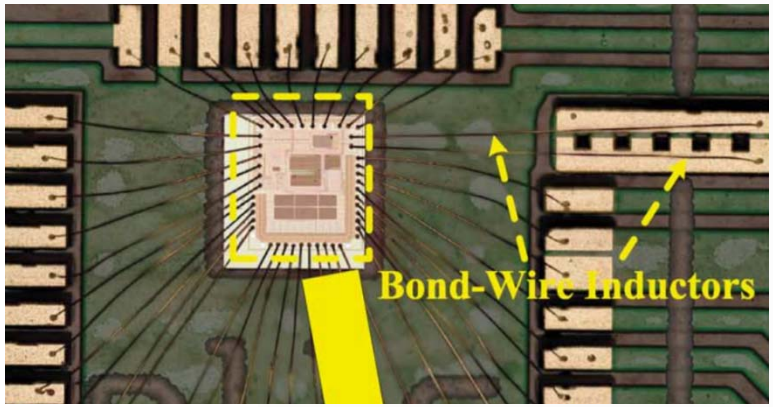
Outline of Lecture #4

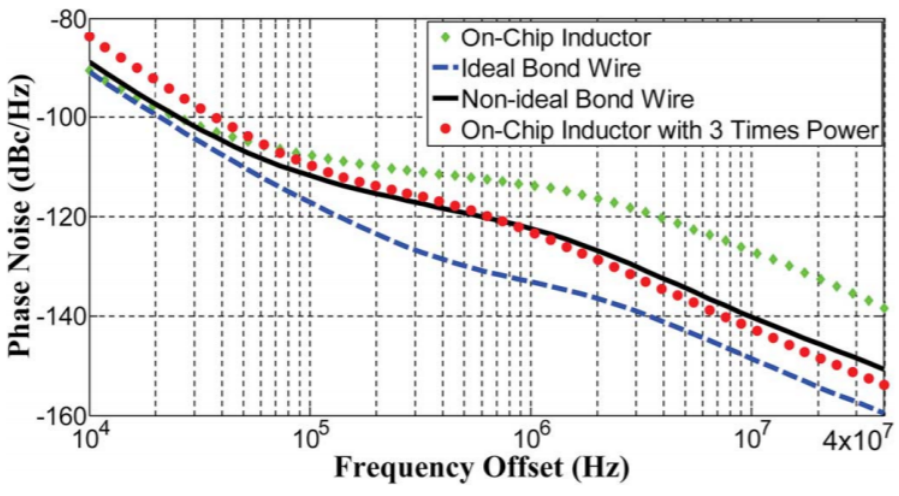
- Parasitic effect in IC design
- Parasitic capacitor & crosstalk
  - Noise Crosstalk between interconnects
  - Parasitic capacitor with Noise & Stability
- Parasitic resistor & grounding issue
  - Grounding (single-point, multi-point)
- Parasitic BJT (Latch-up) protection
  - Parasitic BJT & Latch-up techniques
  - Guard ring technique and Examples
- Utilize Parasitic parameters

Parasitic capacitor #1 (VCO)

- Bond wire inductors and PLLs



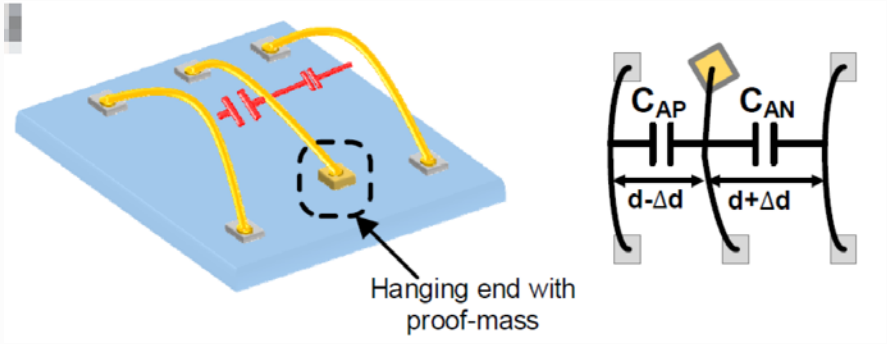


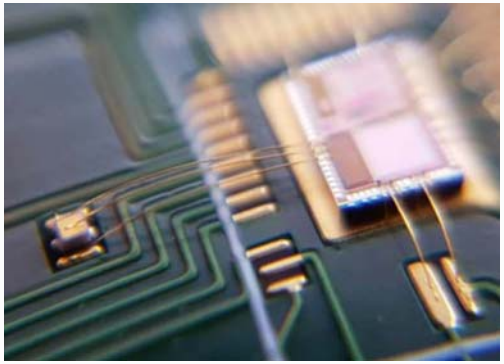


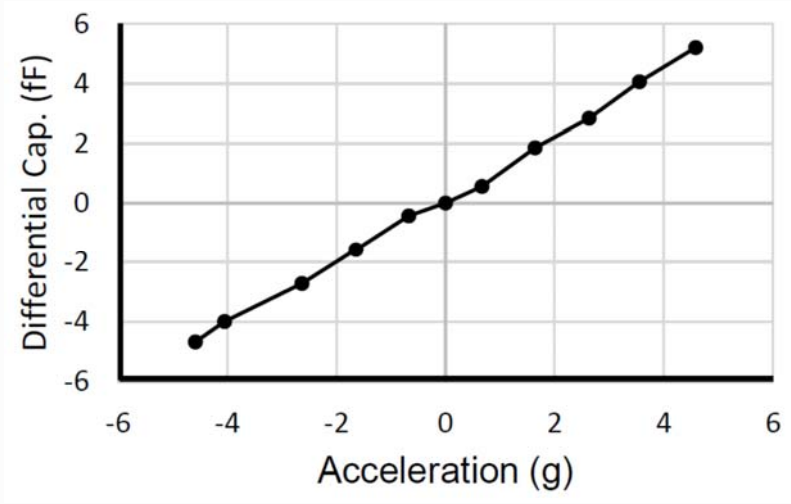
[1] B. Zhao, Y. Lian and H. Yang, "A Low-Power Fast-Settling Bond-Wire Frequency Synthesizer With a Dynamic-Bandwidth Scheme," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 60, no. 5, pp. 1188-1199, May 2013.

Parasitic capacitor #2 (Sensors)

- Bond wire accelerometers (Capacitance mode)
  - Fully differential topology to improve the linearity



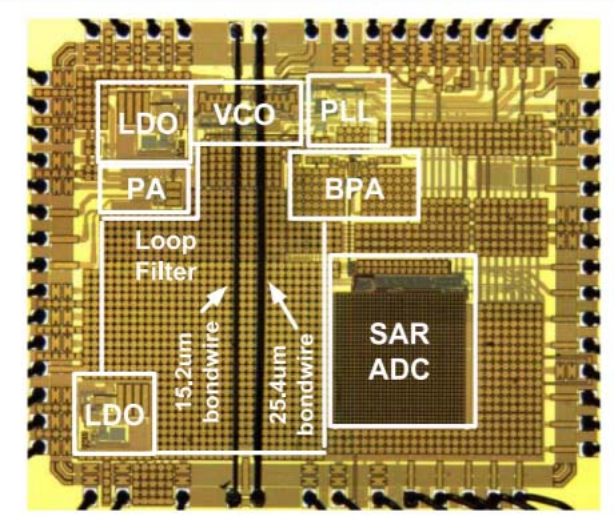


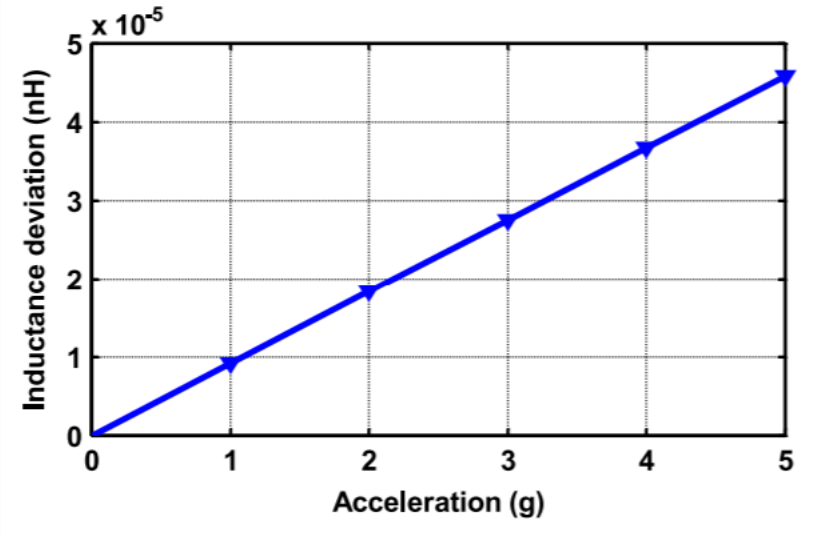


[1] S. Park, G. Lee and S. Cho, "A 2.69 uW Dual Quantization-Based Capacitance-to-Digital Converter for Pressure, Humidity, and Acceleration Sensing in 0.18UM CMOS," 2018 IEEE Symposium on VLSI Circuits, Honolulu, HI, 2018, pp. 163-164.

Parasitic inductor (Sensors)

- Bond wire accelerometers (Inductance mode)

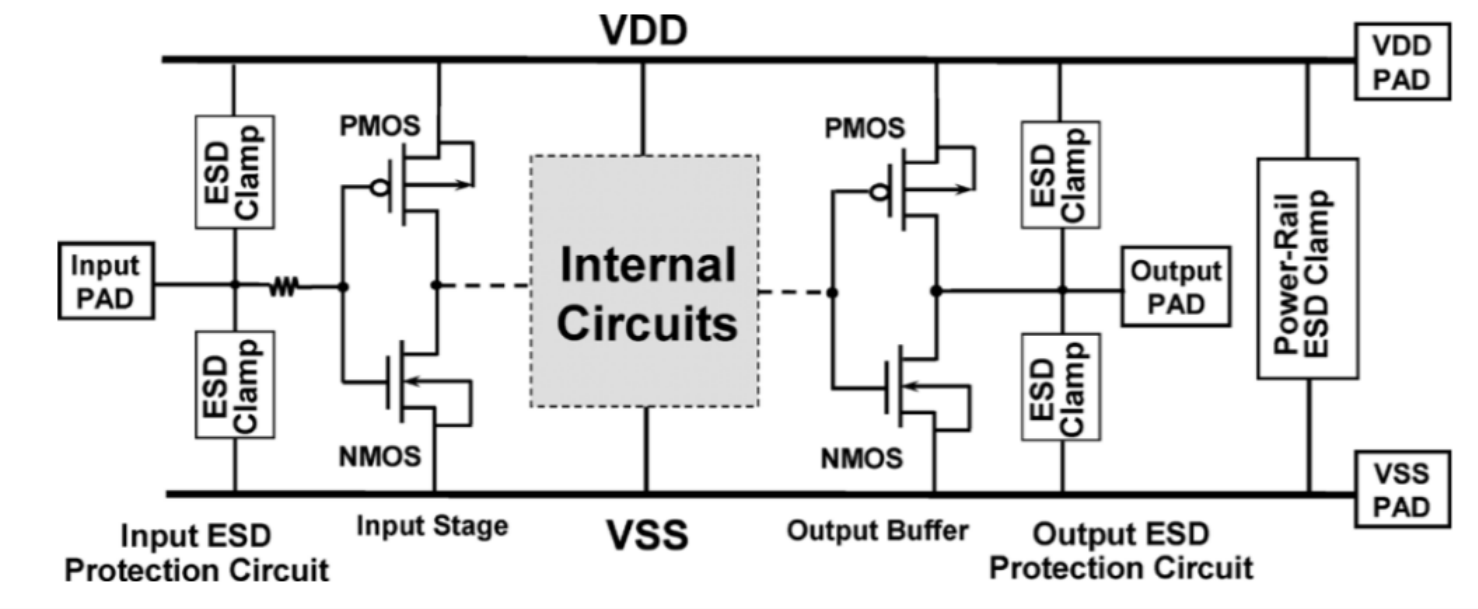




[1] Y. Liao, S. Huang, F. Cheng and T. Tsai, "A Fully-Integrated Wireless Bondwire Accelerometer With Closed-loop Readout Architecture," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 10, pp. 2445-2453, Oct. 2015.

Parasitic BJT (ESD)

- On-chip ESD devices
  - The SCR device can sustain a much higher ESD level within a smaller layout area in CMOS ICs



[1] Overview of On-Chip Electrostatic Discharge Protection Design with SCR-Based Devices in CMOS Integrated Circuits

Summary

- Parasitic effect in IC design
- Parasitic capacitor (inductor) & Shielding
  - Mechanism: Capacitive, inductive
  - Hazards: Off-set, Delay, Noise, Stability…
  - Measures: Shielding, design trade-offs
- Parasitic resistor & Grounding
- Parasitic BJT: Latch-up & Protection
- Utilize parasitic effects

Hint 1: Guard Ring is an useful tool to protect our circuits from parasitic effects!!!

Hint 2: Parasitic effects are not always bad, try to use them in some specific applications!!!

Reminder for next week

- Homework #1
  - Due on May 7th
- Homework #2
  - Due on May 21th