模拟集成电路课程设计（版图）
Layout in Analog Integrated Circuits

Assist. Prof. Jian Zhao
Prof. Guoxing Wang

Shanghai Jiao Tong University
School of Microelectronics
zhaojianycc@sjtu.edu.cn

Instructors

- Time
  - Lecture: Tuesday 14:00 to 15:00
  - Lab: Tuesday 15:00~17:30, Friday 14:00~17:30
- Lecturer
  - Assist. Prof. Jian Zhao (赵健) & Prof. Guoxing Wang
  - School of Microelectronics, Room 427
  - zhaojianycc@sjtu.edu.cn
- Teaching Assistant
  - Dr. Luo Jing (罗京)
  - School of Microelectronics, Room 404.
  - luojing@sjtu.edu.cn

Syllabus (New)

L1: Introduction

L2: Process, Active & Passive Components

L3: Process variation & Matching Issues (匹配问题)

L4: Noise & Shield

L5: Floor planning & Package

L6: Design for Manufacture (Prof. Li Yongfu)

L7: Tracy (Advanced EDA tools by cadence)

L8: Project Review

Review of Lecture #1 & #2

- Introduction of layout
  - What is layout? Why we need layout?
- CMOS process brief
- Introduction of design rules
  - Intra layer rules; Inter layer rules
- Layout of basic cells
  - Active (Transistor), Passive (Resistor, Capacitor)
- Layout design flow
  - Layout, DRC, LVS, PEX

Outline of Lecture #3

- Source of Variations
- Corner Analysis (工艺角分析)
- Random Var., Mismatch (失配) & Monte-carlo
- Deterministic Mismatch
  - Intrinsic & Extrinsic Mismatch
  - Matching for MOSFET (Current & Voltage)
  - Matching for Resistor & Capacitor

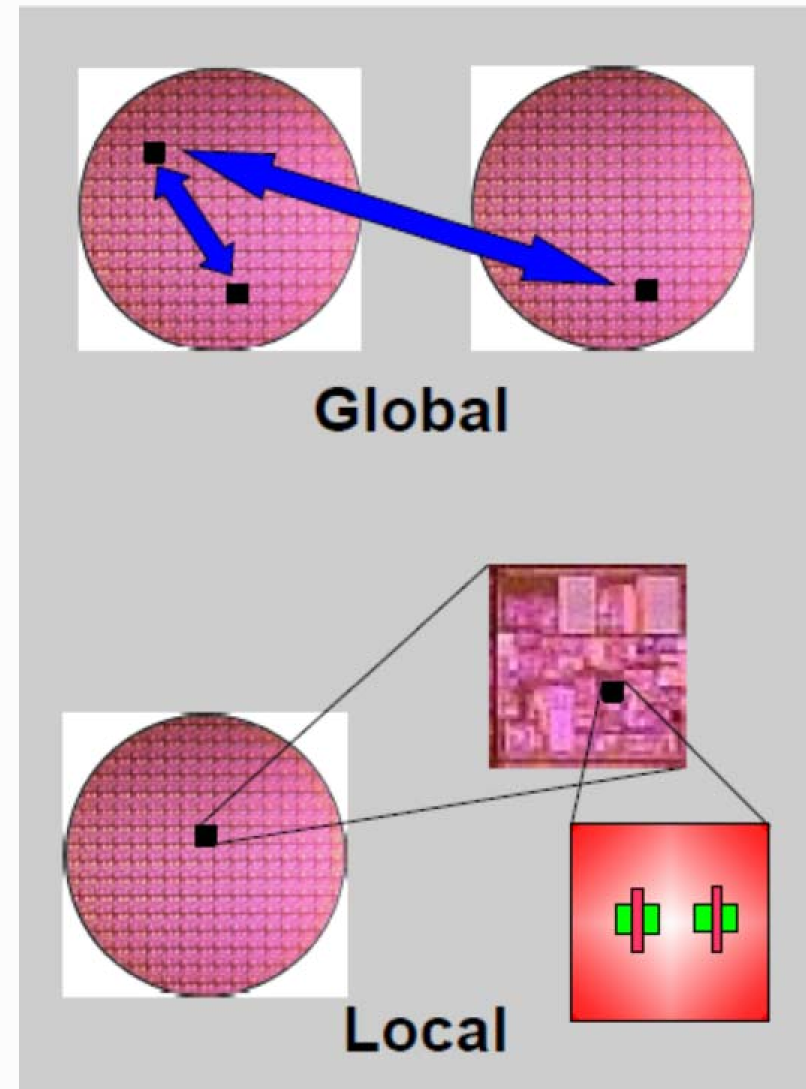
Process Variability

- Process variability become increasingly significant
  - Shrinking devices (W, L, t_{ox})
    - Thin Gate Oxide, Fewer Dopants, sensitive to geometry
  - Higher integrity (Number of devices)
    - Billions of devices per die, higher chance of failure
  - Ultra-low voltage (ΔV_{th})
    - Vth is not scaling by Vdd, Less headroom, more sensitive to ΔV_{th}

$$I_{DS} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2$$

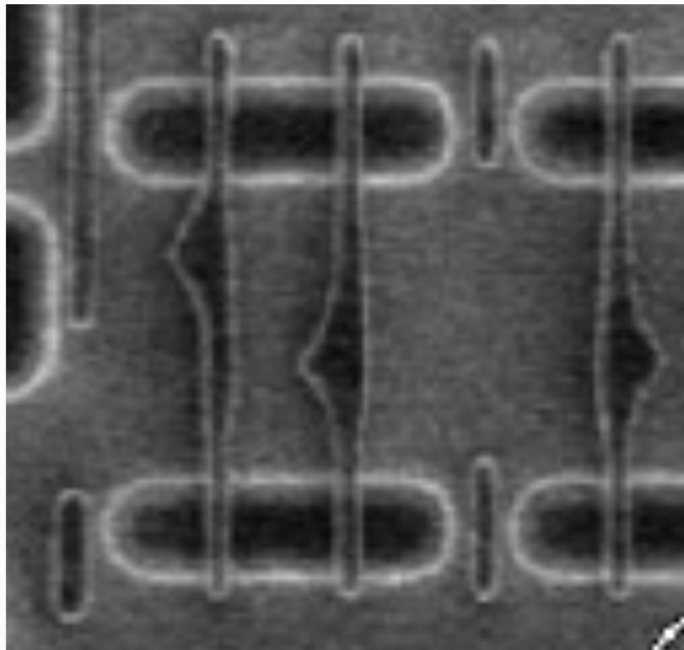
Process variation

- Global: die-to-die, wafer-to-wafer
  - t_{ox} (thickness of oxide)
  - Transistor W & L
  - N/Pwell doping (V_{th})
  - Stress induced effects (V_{th})
- Local: within the die variations
  - Transistor W & L
  - V_{th} mismatch

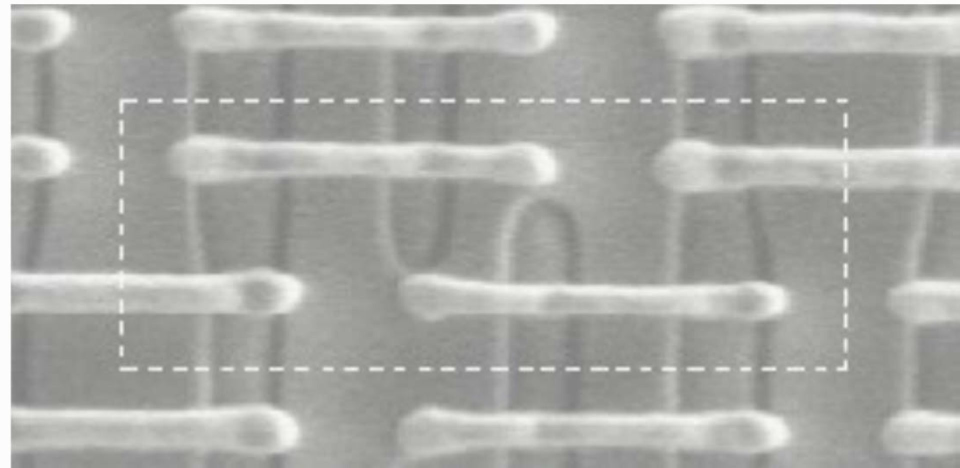


Width and length variations (Geometry)

- Caused by variations in the lithographic process
- Width and Length variations are uncorrelated
- Small transistors more sensitive to W/L changes



65nm CMOS NAND cell

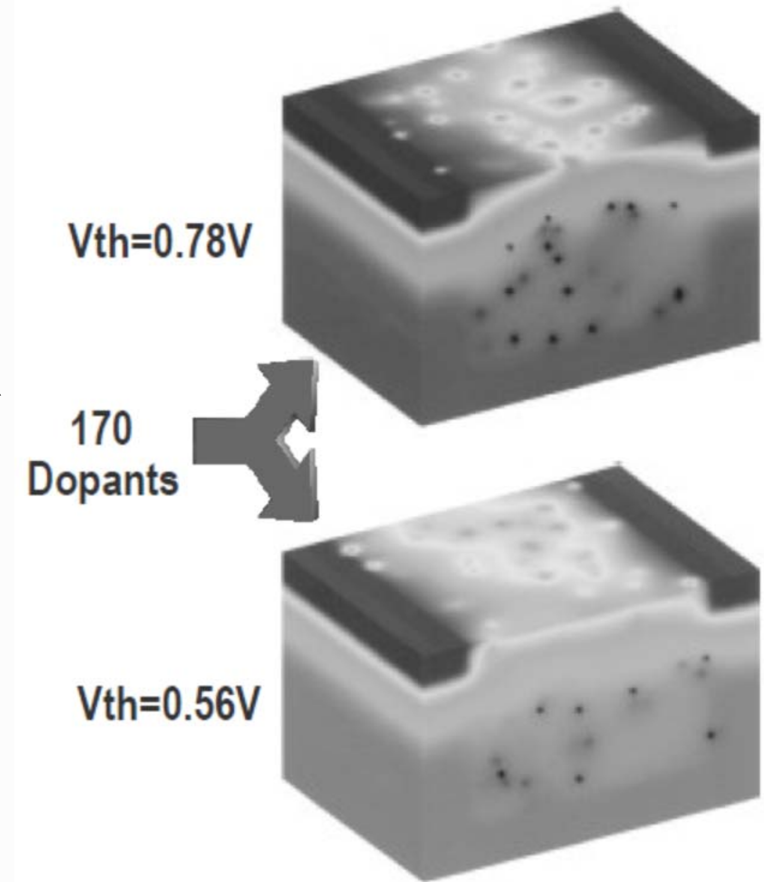


Intel 65nm 6T SRAM cell

V_{th} Variation

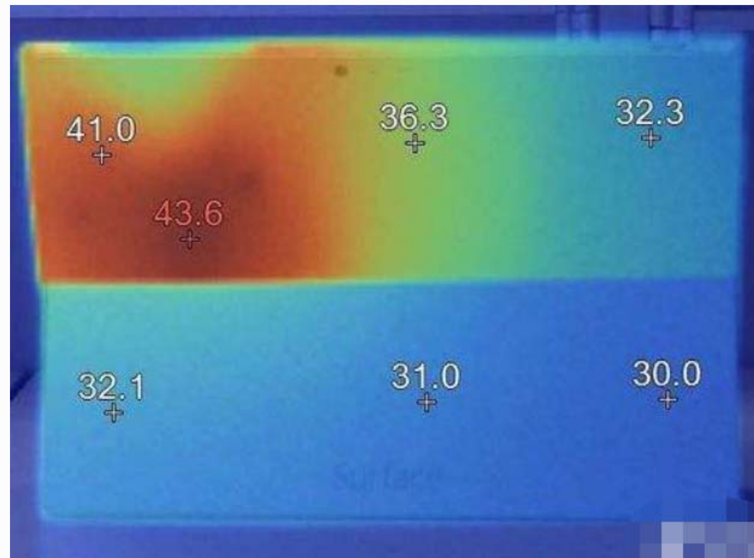
- Random fluctuations due to relatively small number of dopants (掺杂) in the channel.
- V_{th} variance is inversely proportional to transistor area
- Pelgrom's Law:

$$\sigma(V_{th}) = K / \sqrt{W \times L}$$

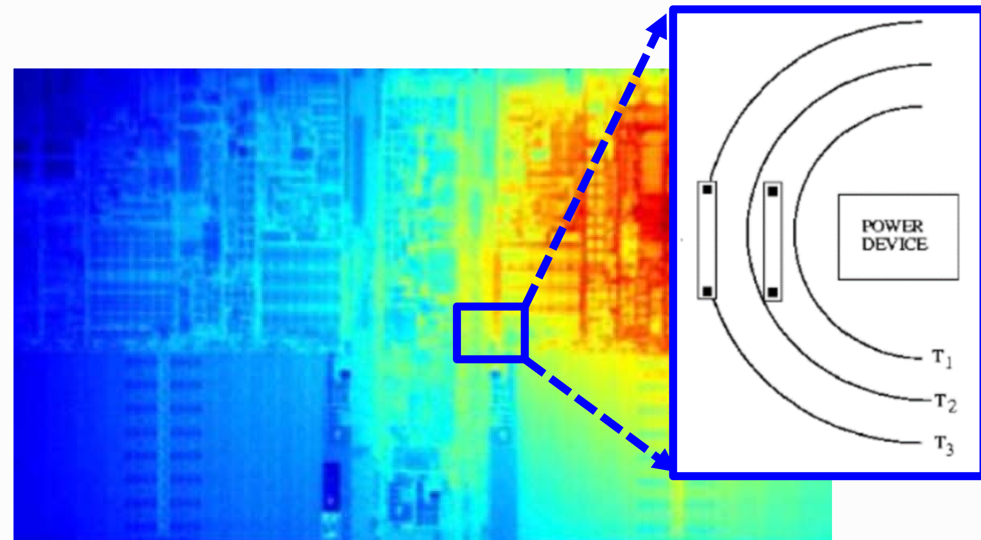


Environmental variations

- Temperature
  - Ambient temperature ranges
  - On-die temperature elevated by chip self-power consumption



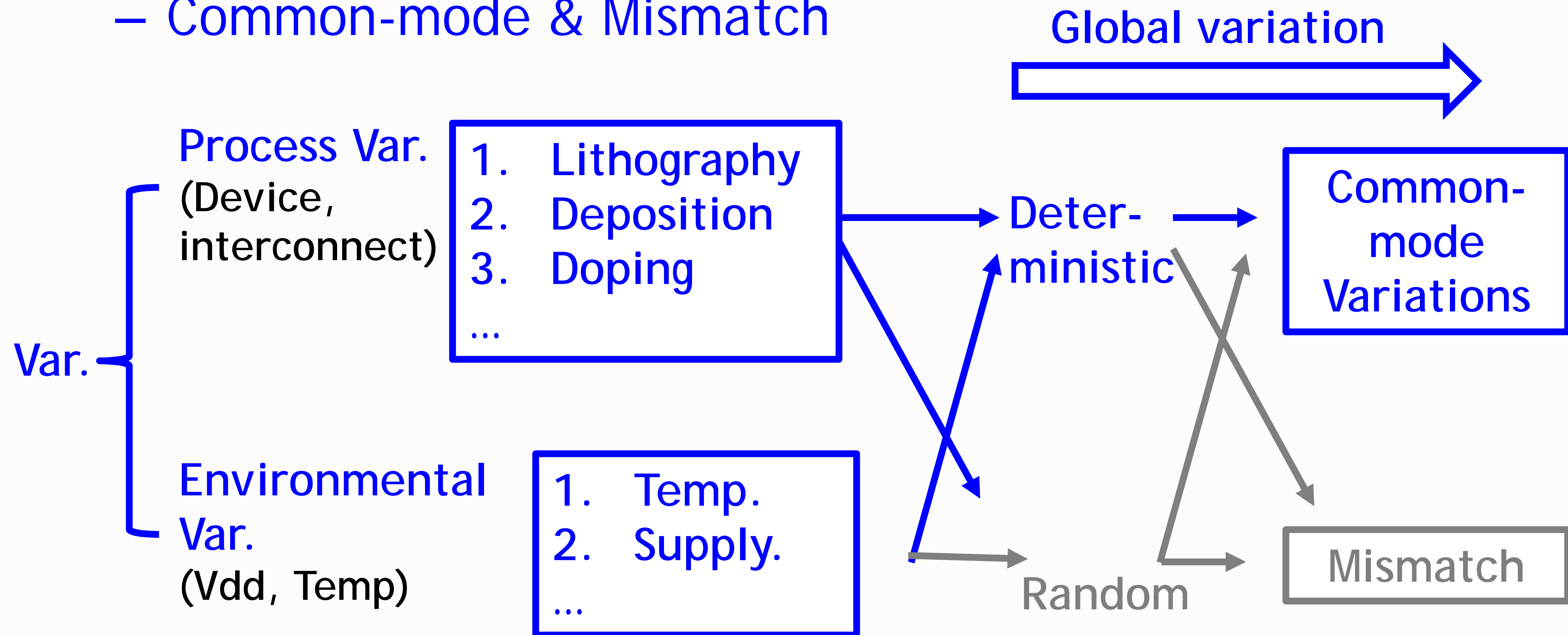
Thermal distribution of a tablet



Thermal distribution of an CPU

Variation classifications

- According to the features
  - Deterministic & Random
- According to the consequence:
  - Common-mode & Mismatch

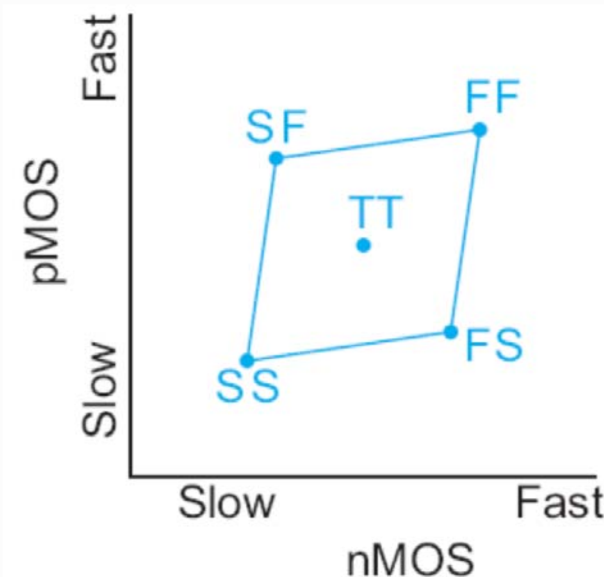


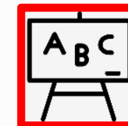
Process Variation & Matching Issue

- Source of Variations
- Corner Analysis 工艺角分析 (PVT analysis)
- Random Var., Mismatch & Monte-carlo
- Deterministic Mismatch
  - Intrinsic & Extrinsic Mismatch
  - Matching for MOSFET (Current & Voltage)
  - Matching for Resistor & Capacitor

Corner analysis for Common-mode Var.

- Model extremes of process variations in simulation
- Corners
  - Typical (T)
  - Fast (F)
  - Slow (S)
- Factors
  - nMOS speed
  - pMOS speed
  - C&R (wire)
  - Voltage
  - Temp.





Continuous & Linear Assumption!

Corner	Voltage	Temperature
F	1.98	0 °C
T	1.8	70 °C
S	1.62	125 °C

Corner analysis for Common-mode Var.

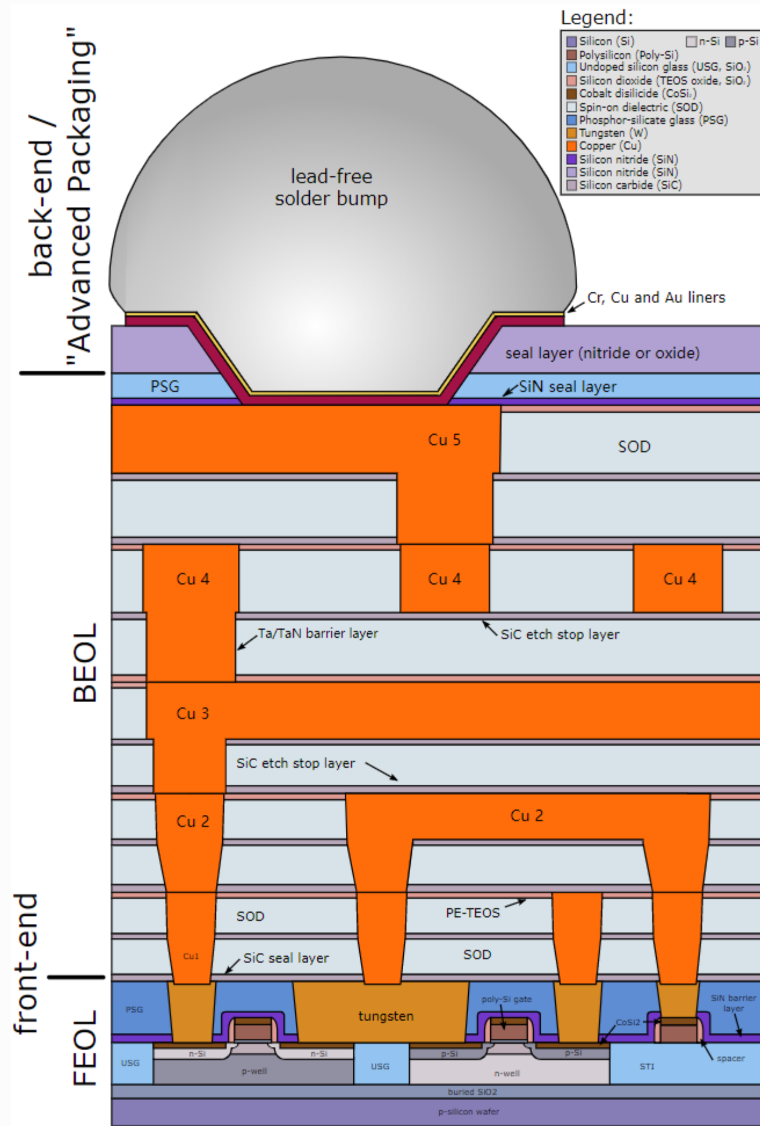
- Circuits are simulated in different corners to verify different performance and correctness specifications

Corner					Purpose
nMOS	pMOS	Wire	V_{DD}	Temp	
T	T	T	S	S	Timing specifications (binned parts)
S	S	S	S	S	Timing specifications (conservative)
F	F	F	F	F	Race conditions, hold time constraints, pulse collapse, noise
S	S	?	F	S	Dynamic power
F	F	F	F	S	Subthreshold leakage noise and power, overall noise analysis
S	S	F	S	S	Races of gates against wires
F	F	S	F	F	Races of wires against gates
S	F	T	F	F	Pseudo-nMOS and ratioed circuits noise margins, memory read/write, race of pMOS against nMOS
F	S	T	F	F	Ratioed circuits, memory read/write, race of nMOS against pMOS

Process (P) Temperature (T)

Voltage (V)

FEOL & BEOL Corners



FEOL

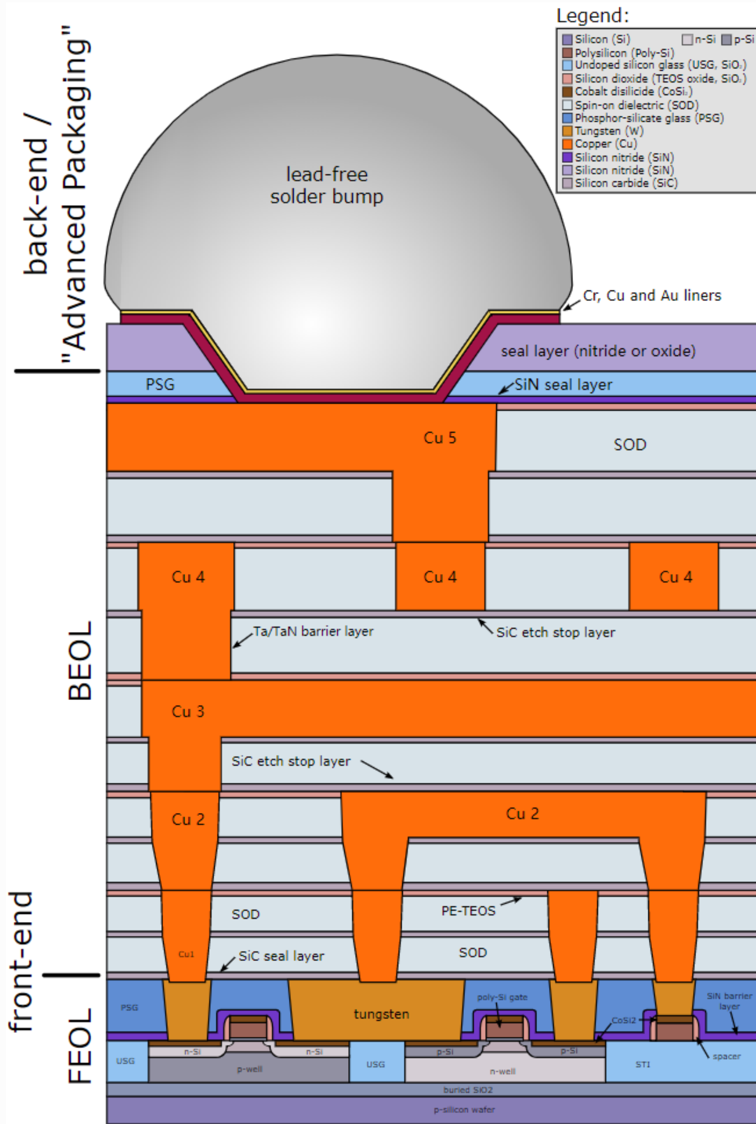
BEOL

0.0	Design grid is 0.25um x 0.25um
1.1	N-well width >= 8um
1.2	N-well spacing and notch >= 8um
2.1	GASAD width >= 2um
2.2	GASAD spacing and notch >= 4um
2.3	N-well enclosure of P-plus active >= 5um
2.4	N-well spacing to N-plus active >= 5um
3.1	Pol
3.2	Pol
3.3	Pol
4.1.a	Pol
4.1.b	Pol
4.2	Pol
4.3	GASAD extension of Poly1 >= 3um
4.4	Poly1 extension of GASAD >= 2.5um
4.5	Poly1 spacing to GASAD >= 1.25um
4.6	Poly0 enclosure of Poly1 >= 3um
5.1	N-plus enclosure of GASAD >= 2.5um
5.2	N-plus spacing to P-plus active >= 2.5um
5.3	N-plus spacing to Poly1 inside P-plus active >= 2um
5.4	N-plus extension of Poly1 inside N-plus active >= 1.5um
5.5	N-plus width >= 2.5um
5.6	N-plus spacing and notch >= 2.5um
6.1	Exact contact size = 2.5um x 2.5um
6.2	Contact spacing >= 3um
6.3	GASAD enclosure of Contact >= 1um
6.4	Poly1 enclosure of Contact >= 1.25um
6.5	Poly1 Contact spacing to GASAD >= 2.5um
6.6	Contact spacing to Poly1 inside GASAD >= 2um
6.9	Poly0 enclosure of Contact >= 4um
6.10	Contact spacing to Poly1 & Poly0 >= 4um
7.1	Metal1 width >= 2.5um
7.2	Met
7.3	Met
8.1	Exa
8.2	Via
8.3	Met
8.4	Via
8.5	Via spacing to Poly1 >= 2.5um
9.1	Metal2 width >= 3.5um
9.2	Metal2 spacing and notch >= 3.5um
9.3	Metal2 enclosure of Via >= 1.25um
10.1	Exact passivation window size = 100um x 100um

Front-end of line
前端工艺

Back-end of line
后端工艺

FEOL & BEOL Corners



FEOL Corner

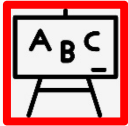
前端工艺角

For MOSFET only
3 Corners: Fast, Typical, Slow

BEOL Corner

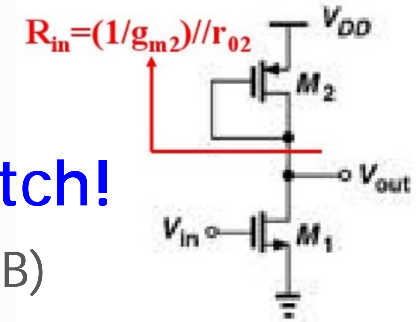
后端工艺角

For Interconnections
For smaller tech. nodes
Process, Voltage, Temperature (PVT)
RC_best, RC_worst



An example of Corner Analysis

- Common source amplifier with diode-type load
- **Differential circuit** is more sensitive to **mismatch!**



DC-Bias (V)

2
1.5
1
0.5
0
TT FF SS FS SF

DC-Bias (V)

DC-Gain (dB)

6
5
4
3
2
1
0
TT FF SS FS SF

DC-Gain

P & N Mismatch

PM (10deg)

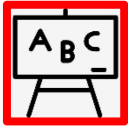
5.8
5.6
5.4
5.2
5
TT FF SS FS SF

PM (10deg)

GBW (MHz)

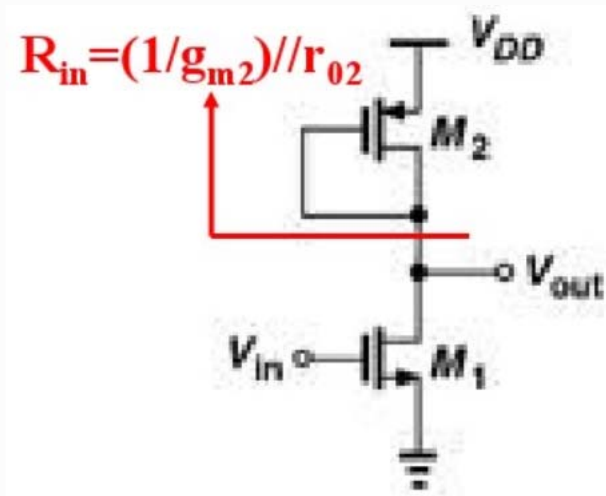
10
5
0
TT FF SS FS SF

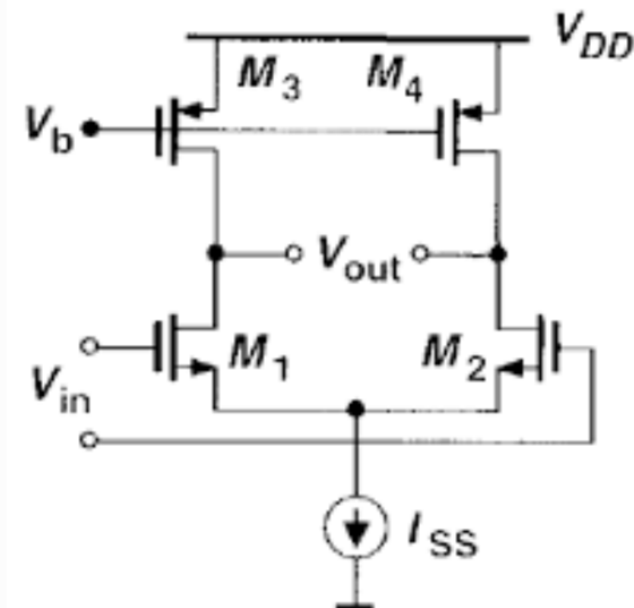
GBW (MHz)



An example of Corner Analysis

- Common source amplifier with diode-type load
- **Differential circuit** is sensitive to **mismatch!**
- Corner can help to check whether all the devices are correctly biased





Single-end

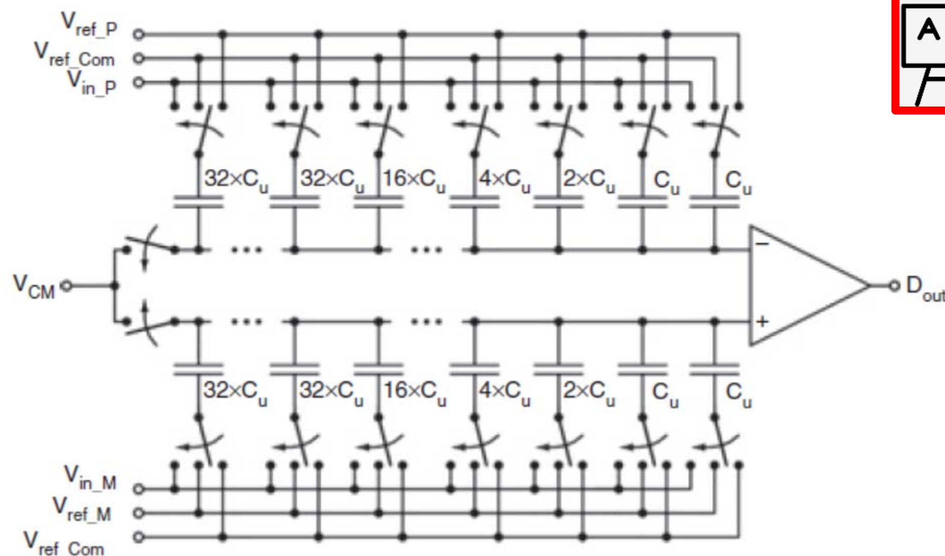
Differential-end

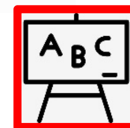
Process Variation & Matching Issue

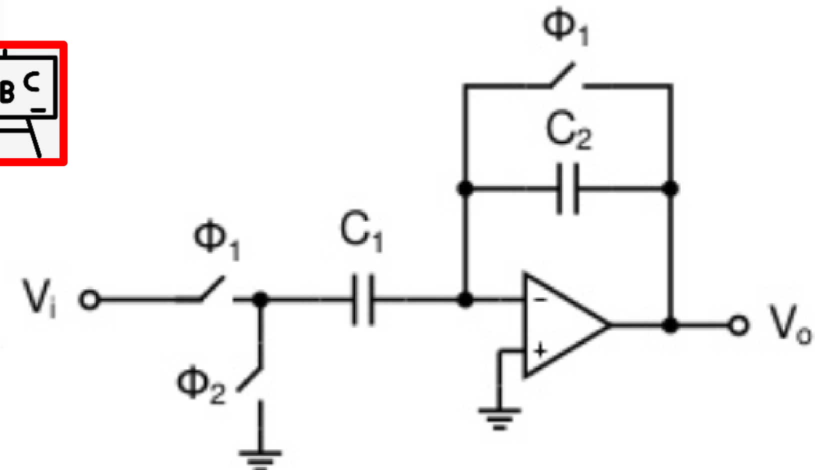
- Source of Variations
- Corner Analysis
- Random Var., Mismatch & Monte-carlo
- Deterministic Mismatch
  - Intrinsic & Extrinsic Mismatch
  - Matching for MOSFET (Current & Voltage)
  - Matching for Resistor & Capacitor

Application of CMOS cap.

- Capacitor array is widely used (ADC, Switch Cap…)
- Capacitor array requires accurate ratio







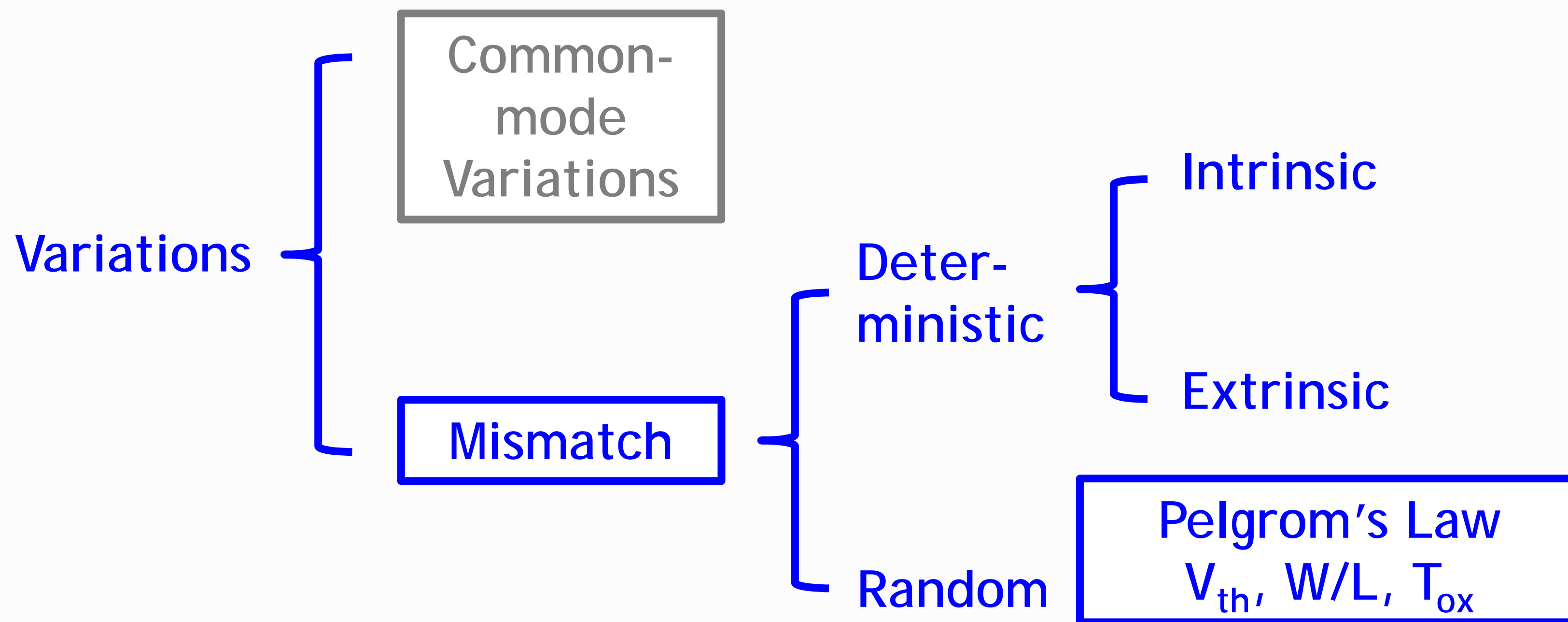
$$H(z) = +\frac{C_1}{C_2} \cdot z^{-1}$$

Capacitors in SAR-ADC

Capacitors in S-C circuit

Variation classifications

- According to the features
  - Deterministic & Random
- According to the consequence:
  - Common-mode & Mismatch

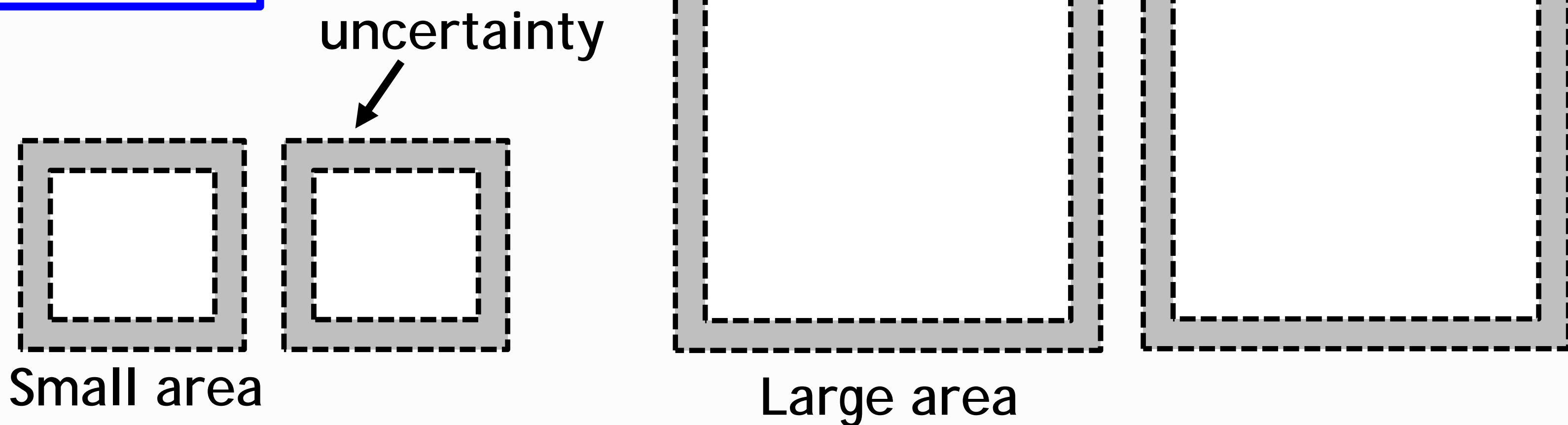


Random Mismatch

- Same with random variations
- Geometry & V_{th} mismatch decrease with area

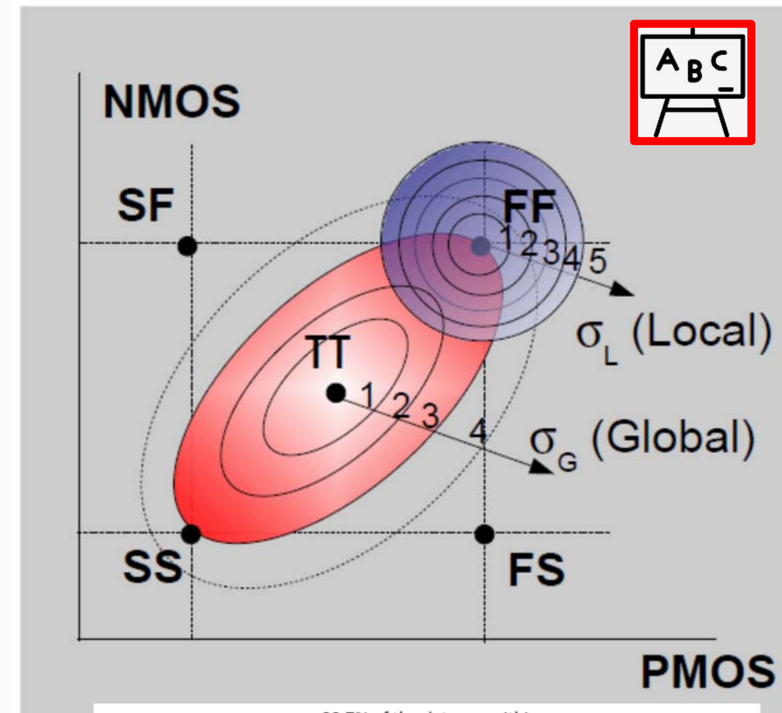
V_{th}:

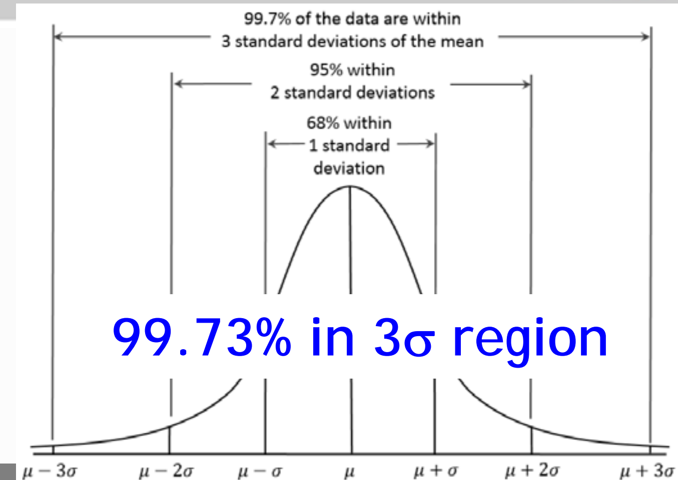
$$\sigma(V_{th}) = K / \sqrt{W \times L}$$



Statistical Models

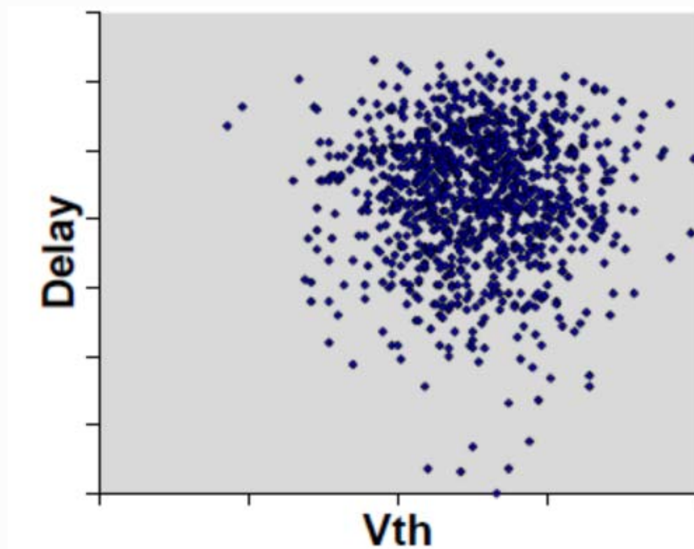
- More realistic than corner models (Corner to bad)
  - Especially when the number of devices is very large
- Can work without linear-continuous assumption
  - Suitable for nonlinear or complex circuit
- Possible to evaluate the mismatch issue

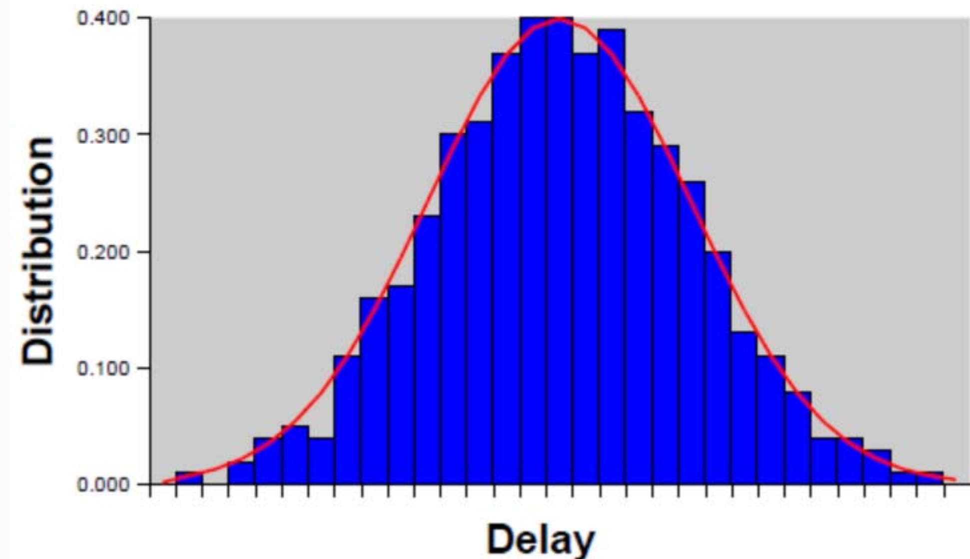




General Concept

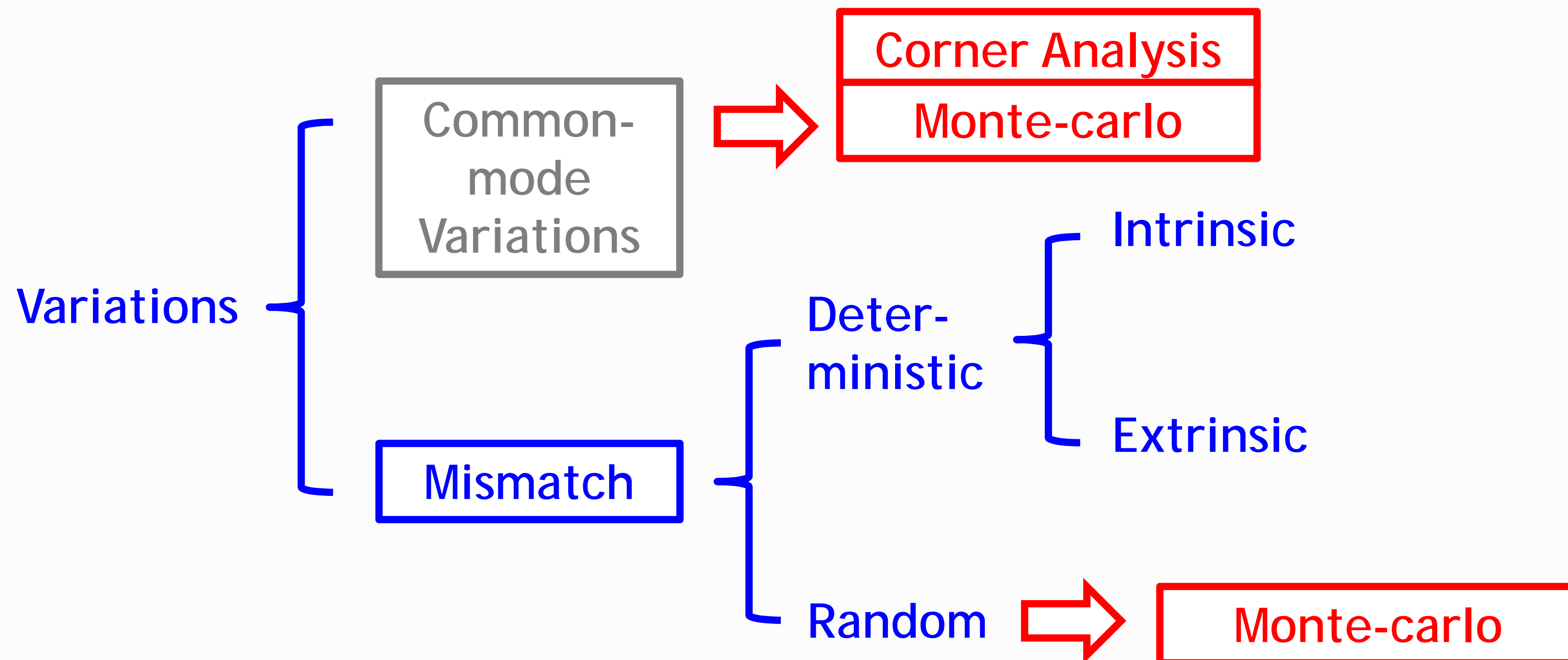
- Monte Carlo involves simulating a circuit over a wide range of randomly chosen devices parameters
- The result is a distribution plot of design constraints, e.g., delay or noise margin (need enough samples)





Variation classifications

- Common mode variations, mismatch
- According to the consequence:
  – Common-mode & Mismatch

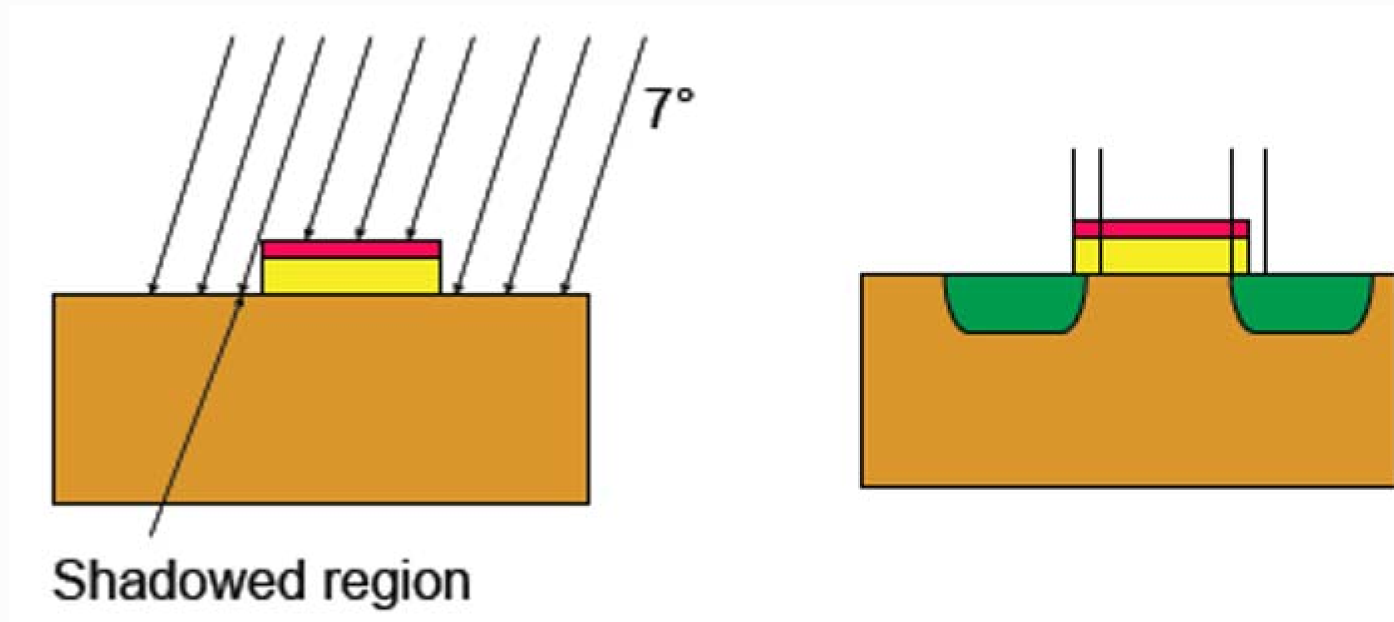


Process Variation & Matching Issue

- Source of Variations
- Corner Analysis
- Random Var., Mismatch & Monte-carlo
- Deterministic Mismatch
  - Intrinsic & Extrinsic Mismatch
  - Matching for MOSFET (Current & Voltage)
  - Matching for Resistor & Capacitor

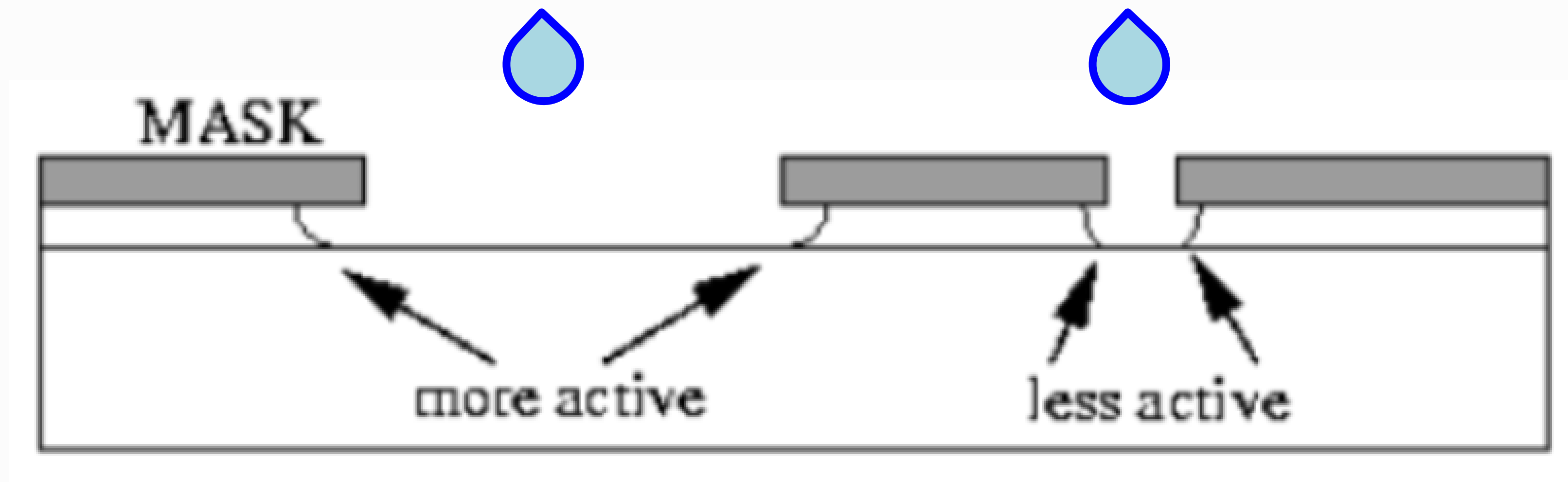
Extrinsic-Anisotropic

- Extrinsic mismatch
  - Annealing (Asymmetry Fabrication)
  - Etching (Undercut, Nonlinear Fabrication)



Extrinsic-Anisotropic

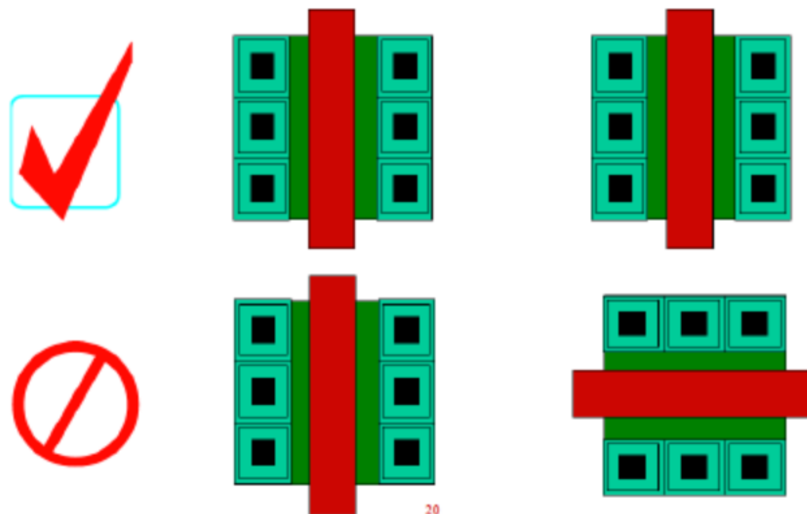
- Extrinsic mismatch
  - Annealing (Asymmetry Fabrication)
  - Etching (Undercut, Nonlinear Fabrication)



Extrinsic-Surroundings

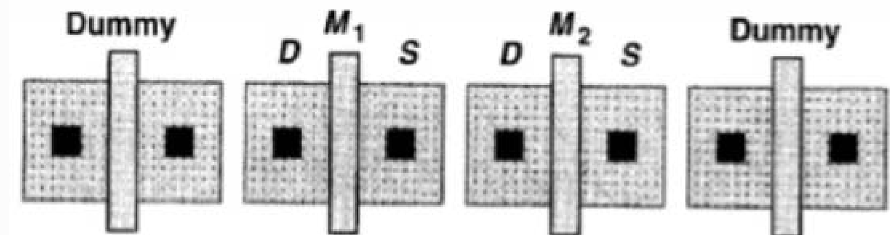
- Extrinsic mismatch
  - Annealing Mismatch (Solution: Direction+Dummy)
  - Etching (Solution: Dummy)

Same Direction



All devices within the die should be in the same direction!

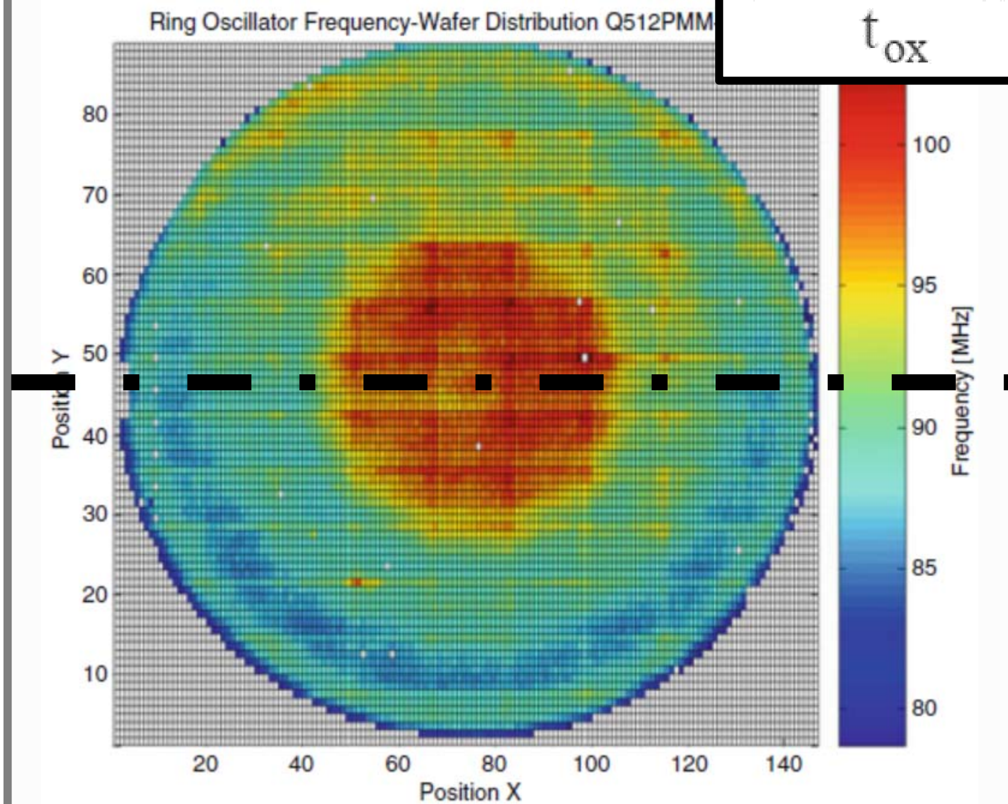
Dummy Block

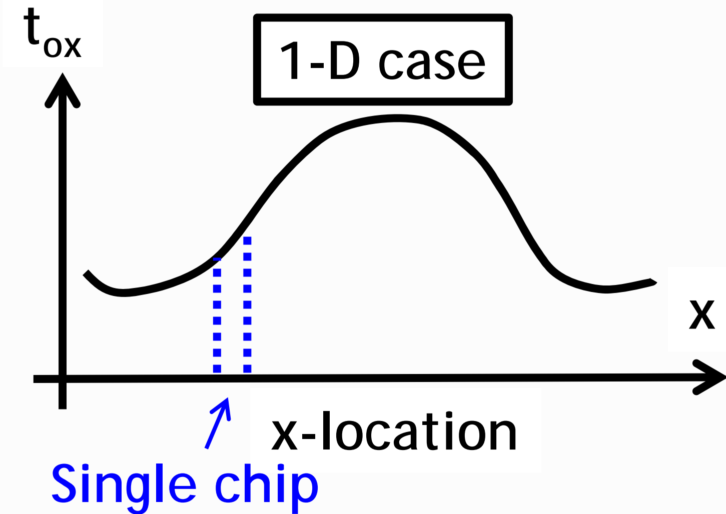


Source of deterministic process error

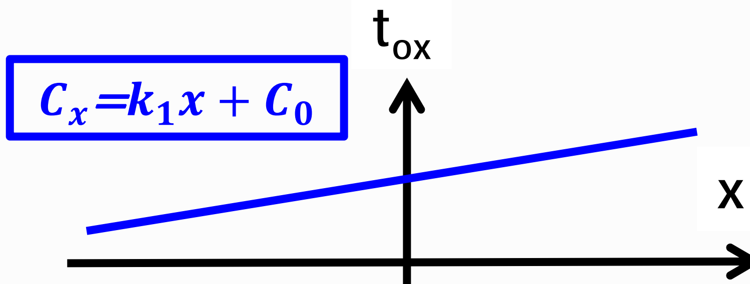
- Polishing seriously affects t_{ox} (within wafer)
- Photolithography are not uniform (within die)

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$



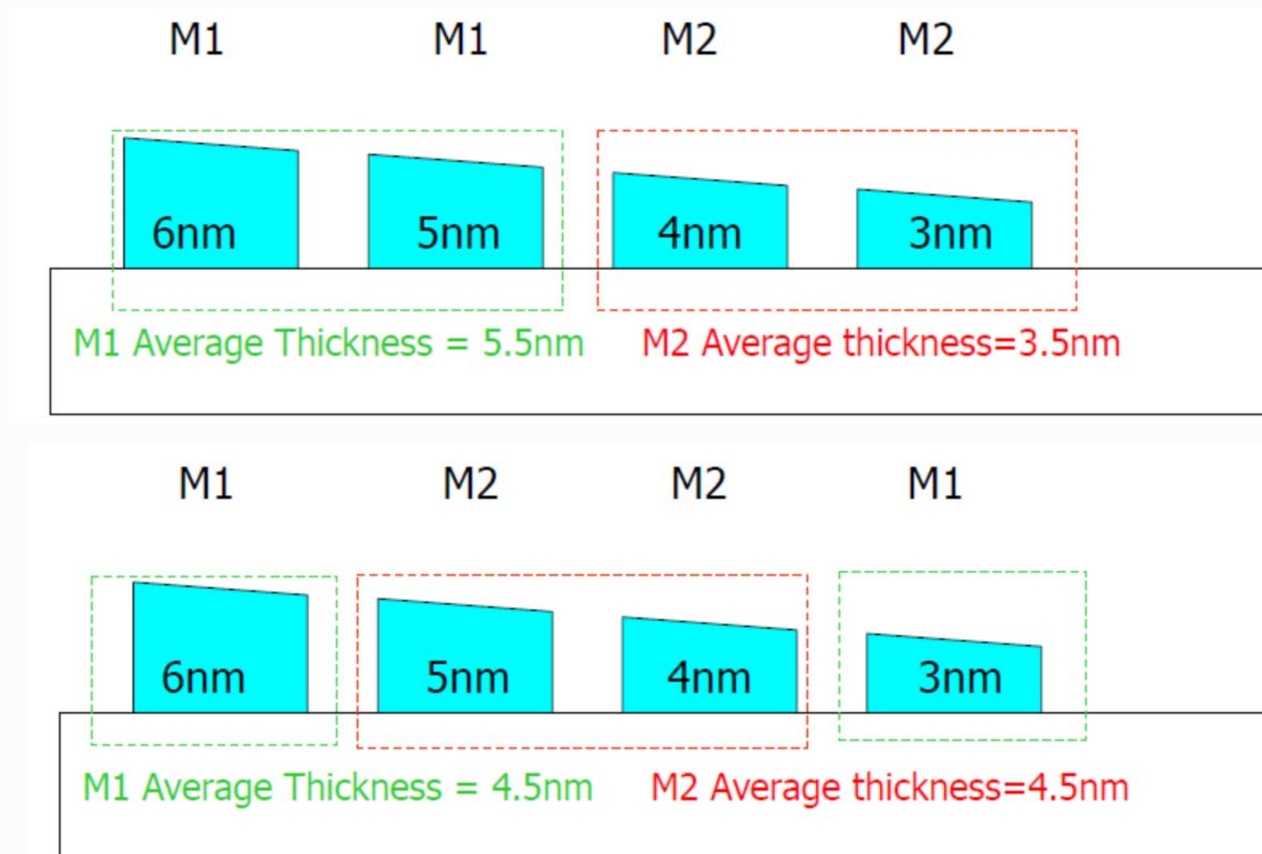


$C_x = k_1 x + C_0$



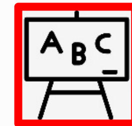
deterministic error cancelling in Layout

- 1st order error cancelling
  - 1D case: symmetrical placement



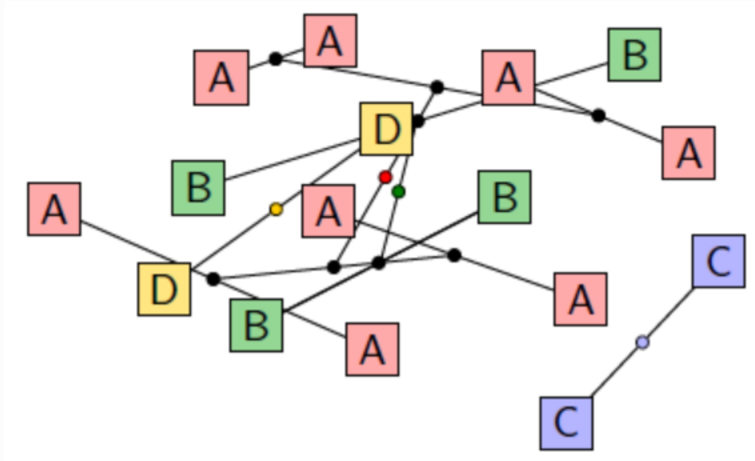
deterministic error cancelling in Layout

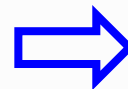
- 1st order error cancelling
  - 1D case: symmetrical placement
  - 2D case: centroid placement & Coincidence

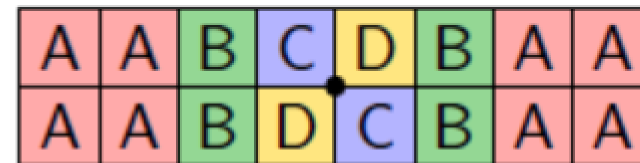


Example: A:B:C:D=4:2:1:1

$$P_x = k_2 x^2 + \boldsymbol{k_1 x} + P_0$$



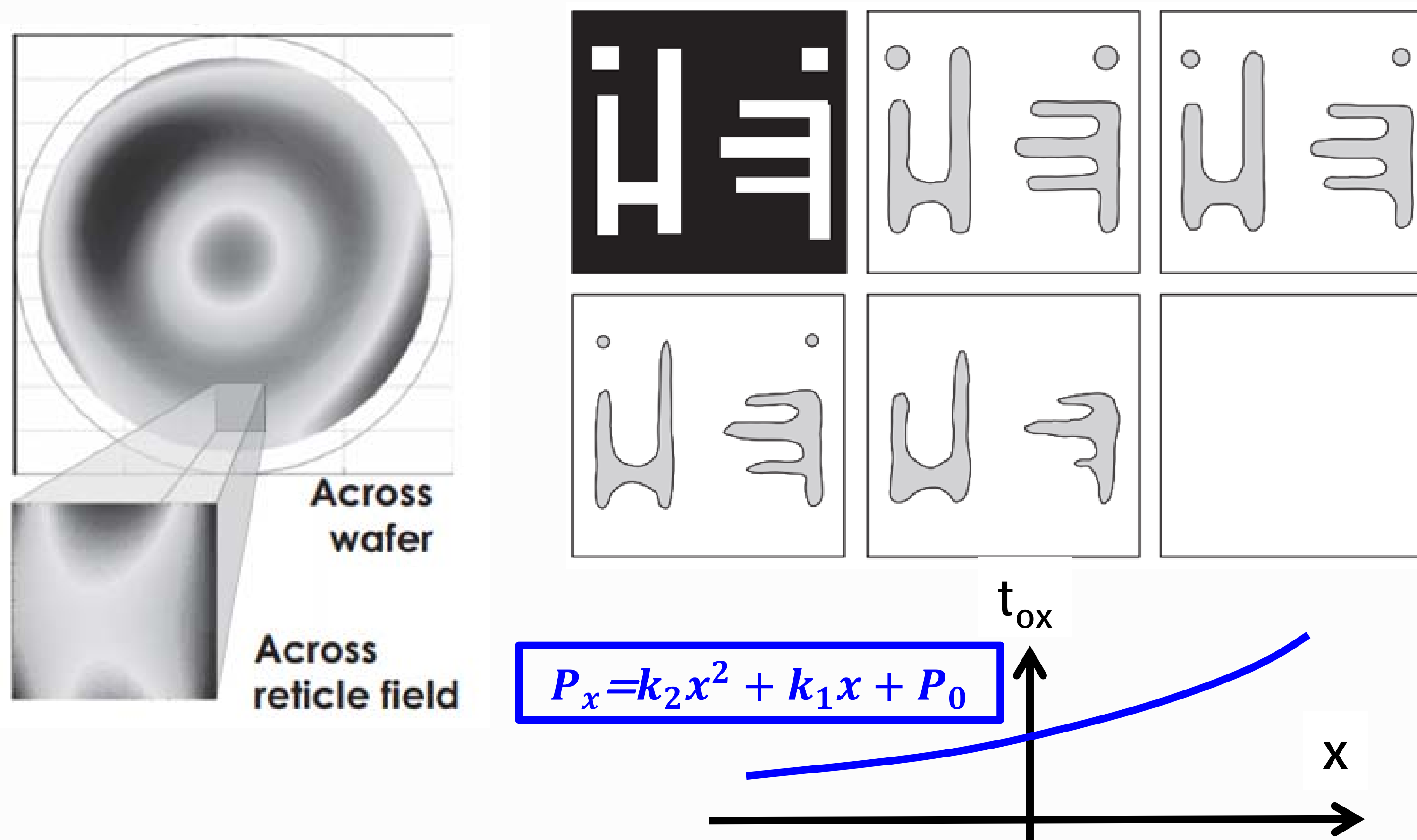




Small t_{ox} ⟹ large t_{ox}

Source of deterministic process error

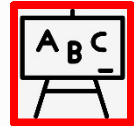
- Polishing seriously affects t_{ox} (within wafer)
- Photolithography are not uniform (within die)



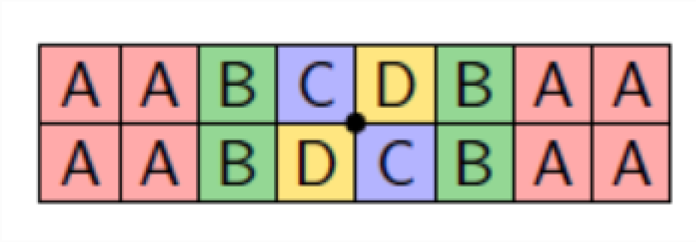
deterministic error cancelling in Layout

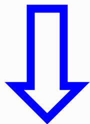
- 2nd order error reduction (difficult to be cancelled)
  - Dispersion (交错排列)
  - Compactness (紧凑排列)

$$P_x = \boldsymbol{k_2 x^2} + k_1 x + P_0$$

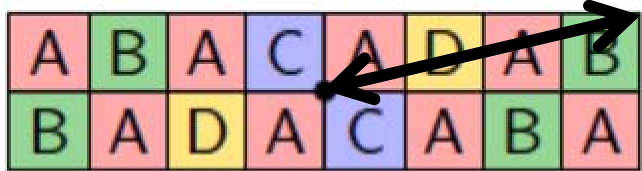


Large distance = large error!

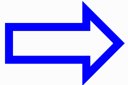




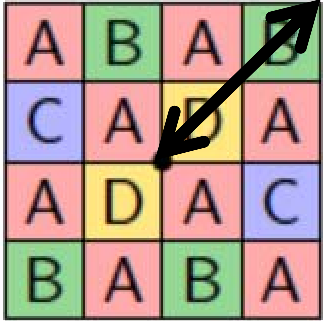
D_{max}=4.12



Dispersion



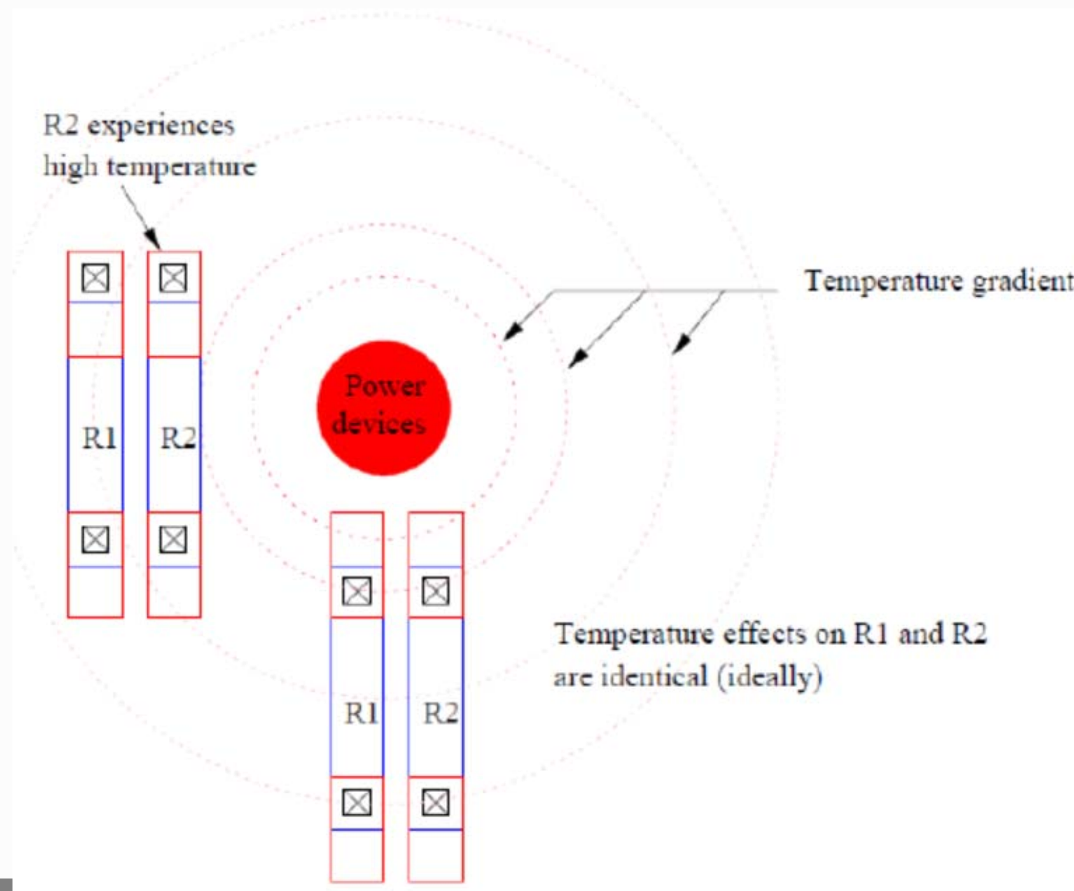
D_{max}=2.8



Compact

Intrinsic Mismatch (Environmental)

- Temperature effect is similar to process var.
- Single source generates 1st order var., Multi-source generates higher order var.



Process Variation & Matching Issue

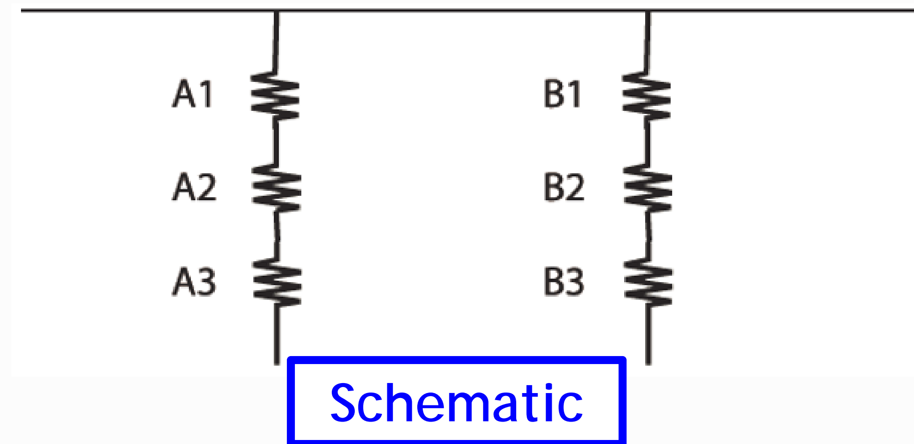
- Source of Variations
- Corner Analysis
- Random Var., Mismatch & Monte-carlo
- Deterministic Mismatch
  - Intrinsic & Extrinsic Mismatch
  - Matching for MOSFET (Current & Voltage)
  - Matching for Resistor & Capacitor
  - (Additional) Few examples

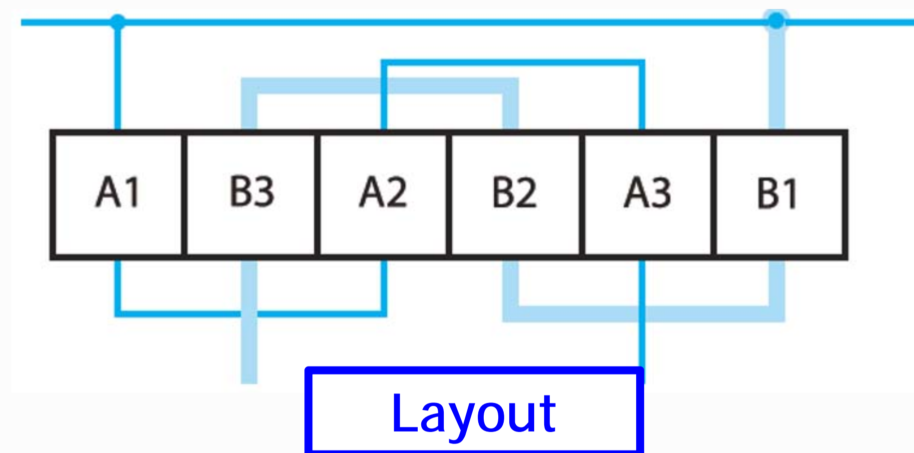
Rule of thumb in Analog layout

- Symmetry
  - Axial symmetry (1-D), Centroid (2-D), dummy, direction
- Dispersion
  - Interdigitated
- Compact

Interdigitated Layout for Transistors & Res.

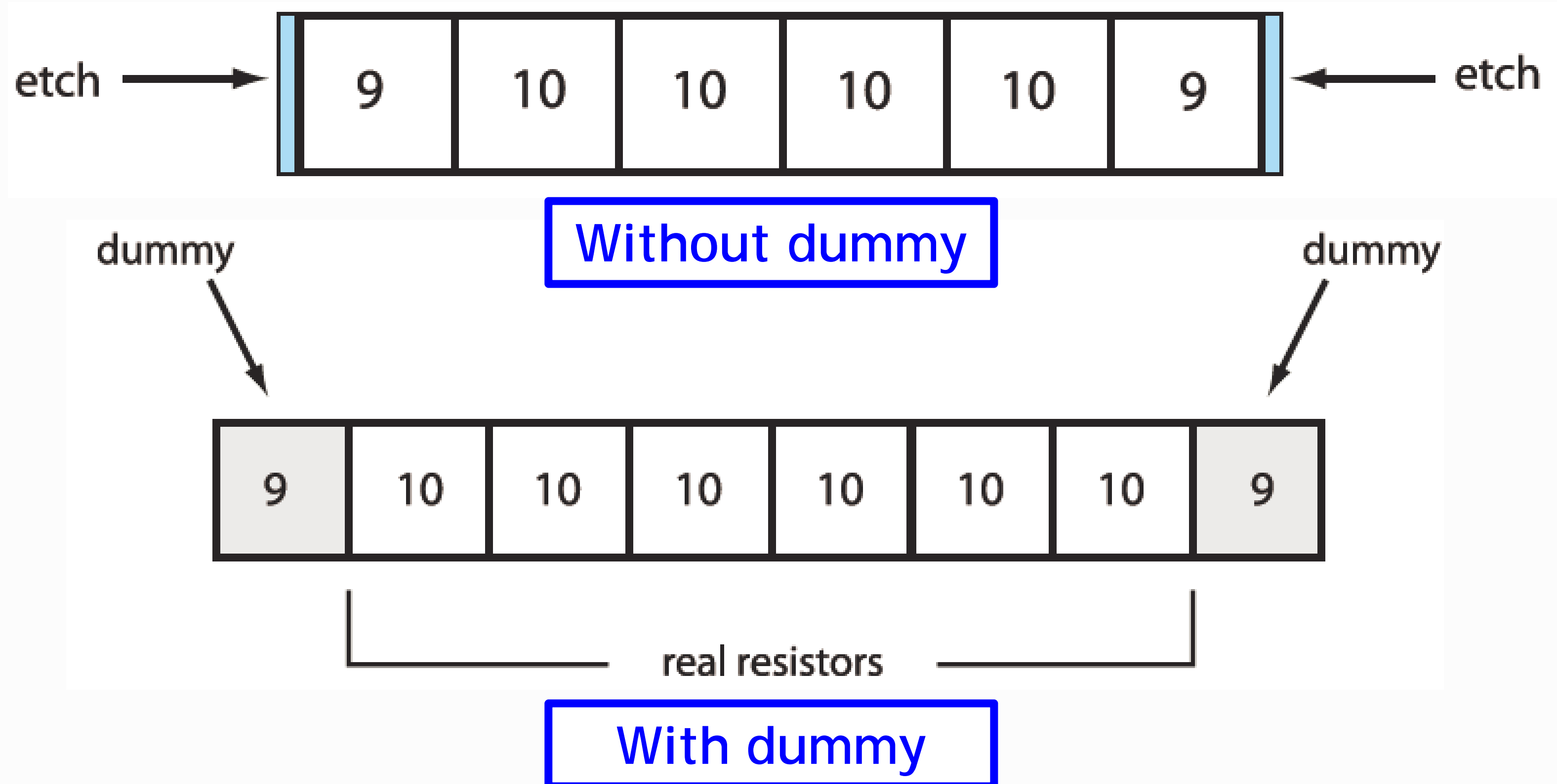
- Interdigitated components for better matching





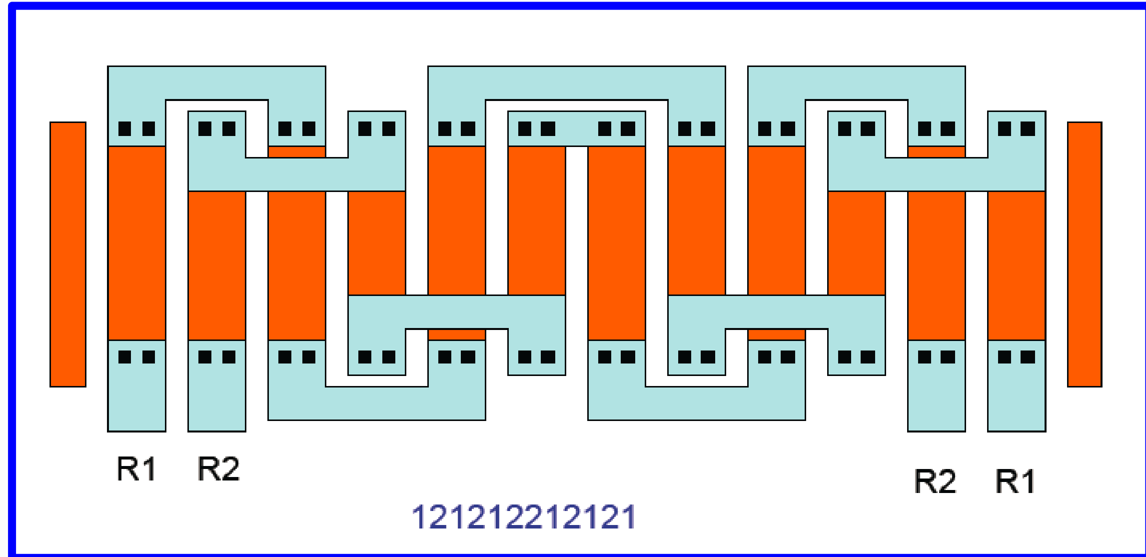
Dummy for active & passive devices

- Dummy block for to achieve identical surroundings.

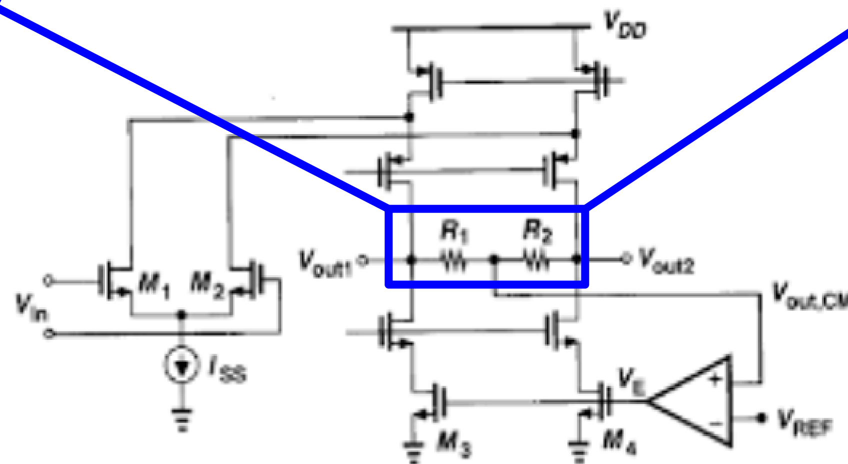


Example layout (1D matching)

- Interdigitating with dummy for better matching.
- Ex. Common-mode feedback circuit

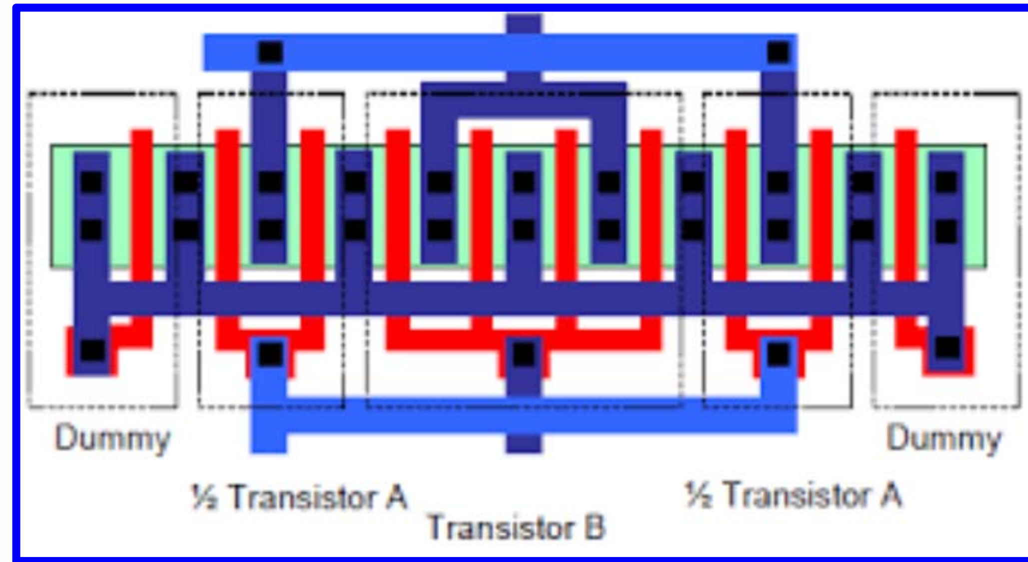


Symmetry?
Dispersion?
Compact?

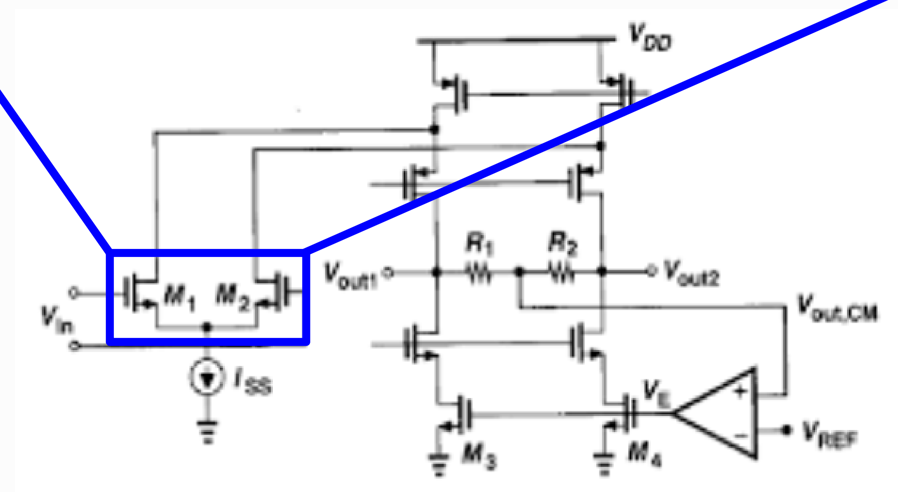


Example layout (1D matching)

- Interdigitating with dummy for better matching.
- Ex. Input pair of an opam

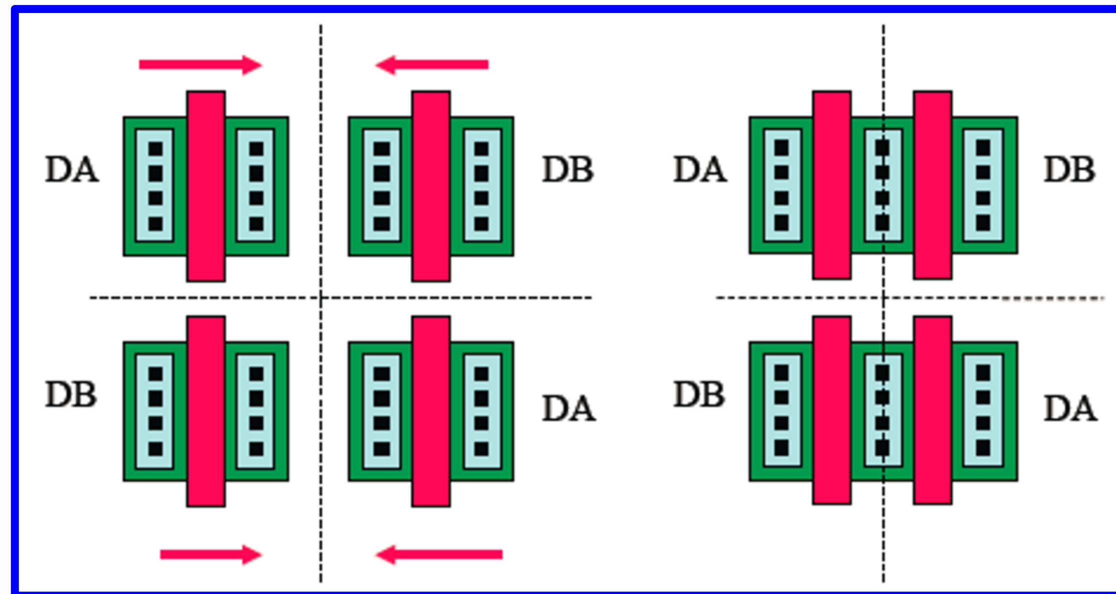


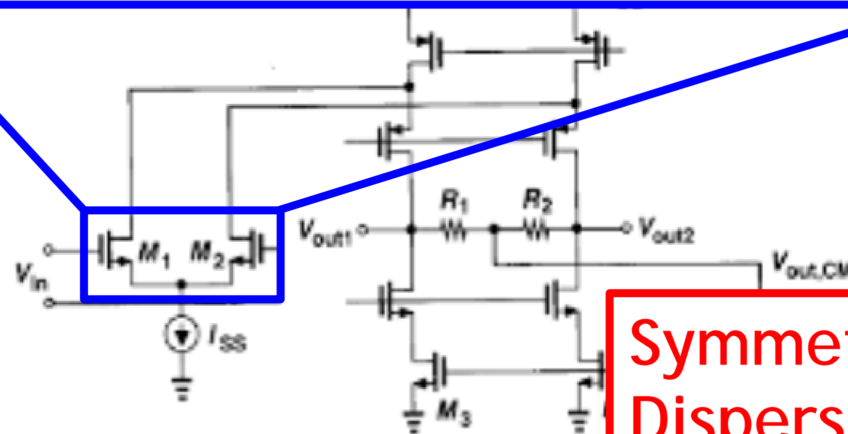
Symmetry?
Dispersion?
Compact?



Example layout (2D matching)

- Centroid layout can cancel the 1st order deterministic error.
- Ex. Input pair of an opam
- However it introduces the complexity of wiring.

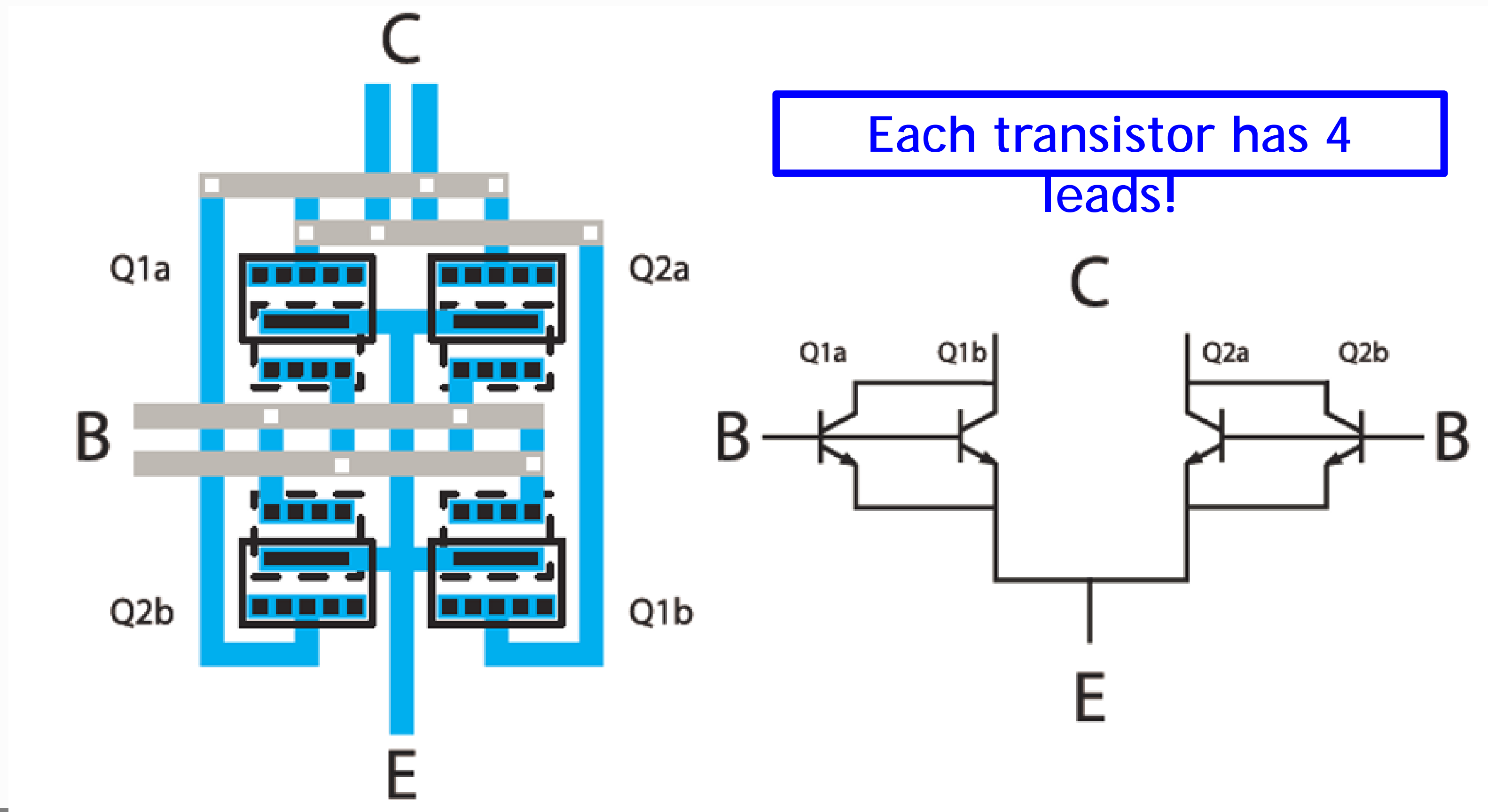




Symmetry?
Dispersion?
Compact?

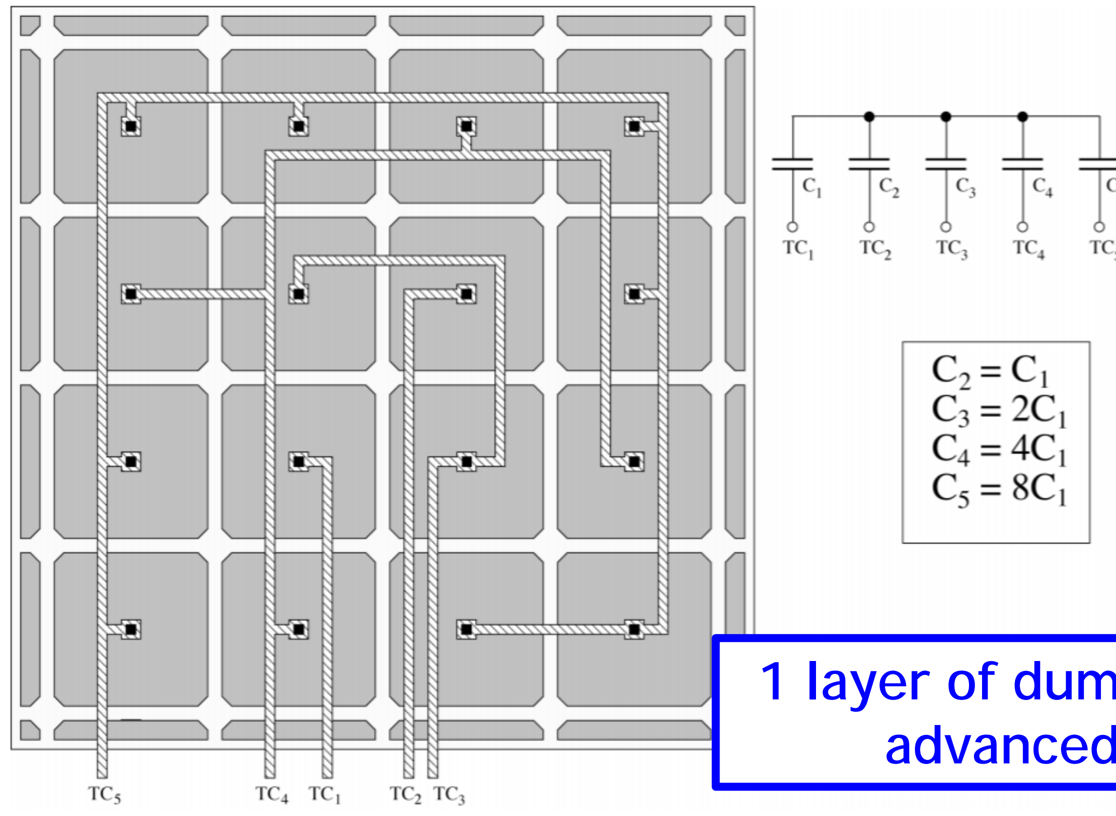
Wiring for centroid MOSFETs

- Wiring for centroid MOSFETs is difficult
- Extra- overlaps in the connector and base wiring (dummy)
- Same length, same metals, same overlaps



Layout and wiring for cap. array

- Centroid + dummy cap. to cancel the deterministic error.
- Ex. SAR ADC cap. array



Symmetry?
Dispersion?
Compact?

1 layer of dummy is not enough in advanced technology !!!

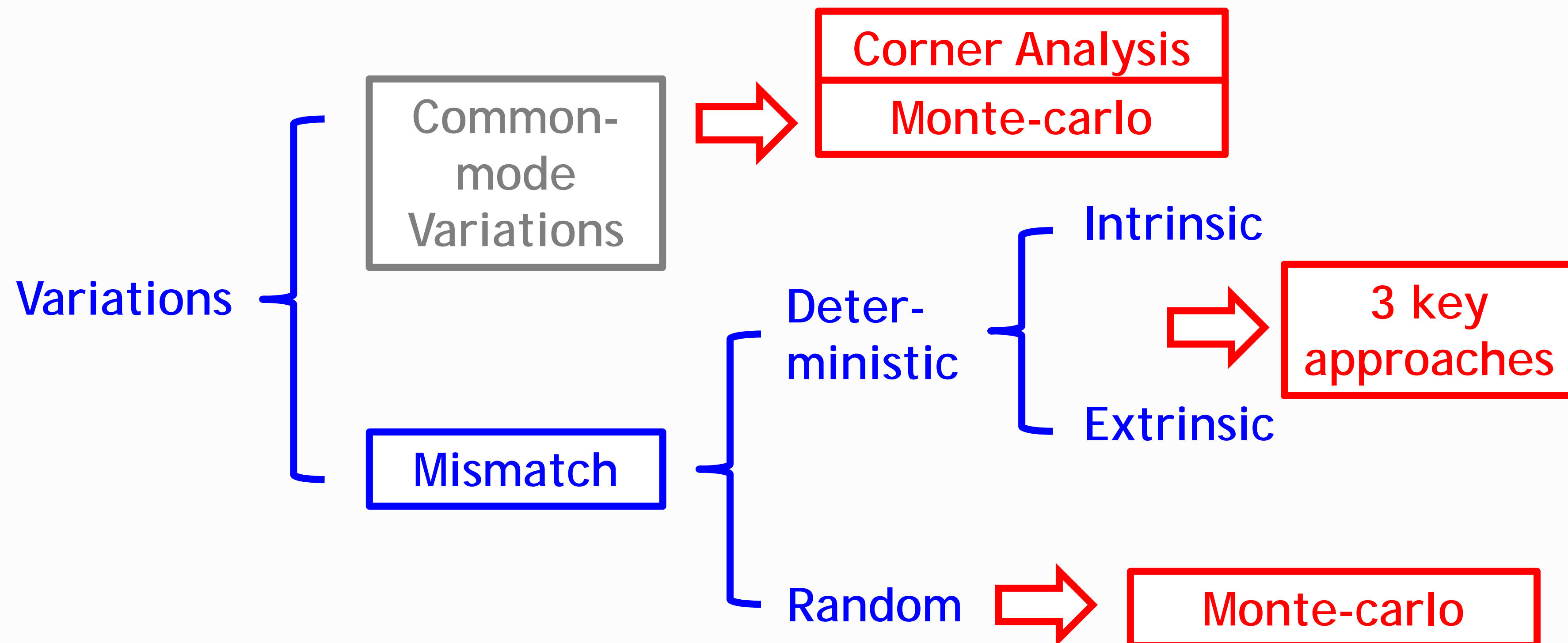
Summary

- Source of Variations
  - Geometry, V_{th}, Environment
- Corner Analysis
- Random Var., Mismatch & Monte-carlo
- Deterministic Mismatch
  - Intrinsic & Extrinsic Mismatch
  - Examples for layout matching

Better understanding requires more practice !!!

Variation classifications

- Common mode variations, mismatch
- According to the consequence:
  - Common-mode & Mismatch



Reminder for next week

- Homework #1
  - Due on May 7th
- Homework #2
  - Corner of monte-carlo simulation (pre-layout, post-layout)