模拟集成电路课程设计（版图）
Layout in Analog Integrated Circuits

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Instructors

- Time
  - Lecture: Tuesday 14:00 to 15:00
  - Lab: Tuesday 15:00~17:30, Friday 14:00~17:30
- Lecturer
  - Assist. Prof. Jian Zhao (赵健) & Prof. Guoxing Wang
  - School of Microelectronics, Room 427
  - zhaojianycc@sjtu.edu.cn
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  - School of Microelectronics, Room 404.
  - luojing@sjtu.edu.cn

WeChat group

MR413模拟集成电路课程设计

该二维码7天内(4月30日前)有效，重新进入将更新

Syllabus

L1: Introduction

L2: Process, Active & Passive Components

L3: Process variation & Matching Issues

L4: Parasitic Effects

L5: Noise & Shield

L6: Failure Mechanism & DFM

L7: Floor planning & Package

L8: Layout of Amplifiers & Data Converters

Grade

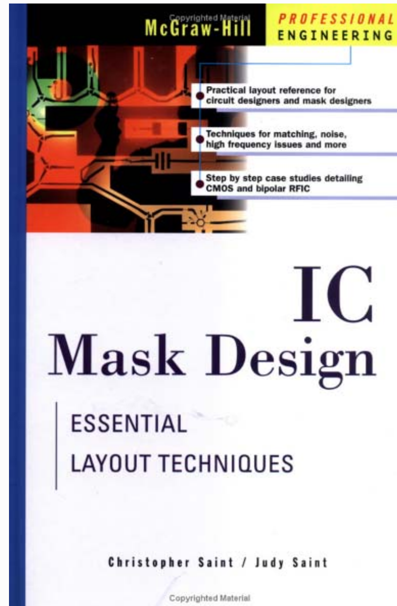
- Home work assignments : **40% (10+15+15)**
- Class performance: **20%** (10% for attendance)
- One project : **40%**

No copy from others!

Students are encouraged to provide feedbacks after each course~

Website of this module is in progress…

Textbook & Materials



IC Mask Design Essential Layout Techniques,
Christopher Saint, et al.,
McGraw Hill, 2002

The Art of Analog Layout,
Alan Hastings,
Pearson Education, 2006

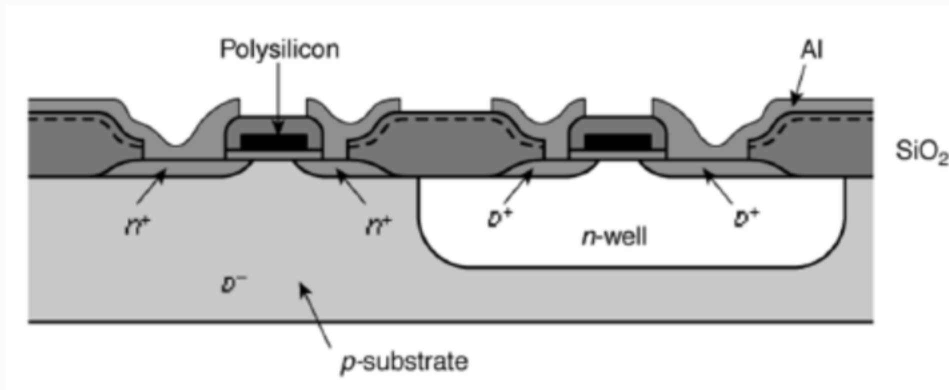
[1] Layout of Analog CMOS Integrated Circuits, Franco Malberti.
www.ims.unipv.it/Courses/download/AIC/
[2] CMOS Transistor Layout KungFu , Lee Eng Han, 2005. www.eda-utilities.com

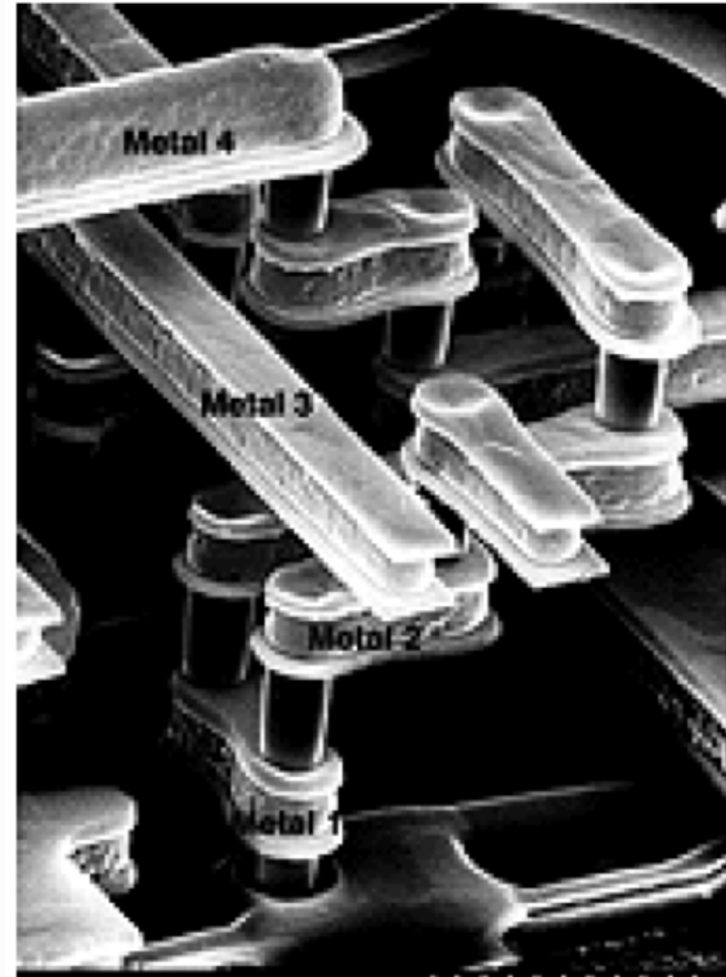
Outline of lecture 1 & 2

- Introduction of Analog Layout
- CMOS process brief
- Design rules
- Basic cells layout
- Design flow of Analog layout (DRC, LVS, PEX)

IC-connecting billions of transistors

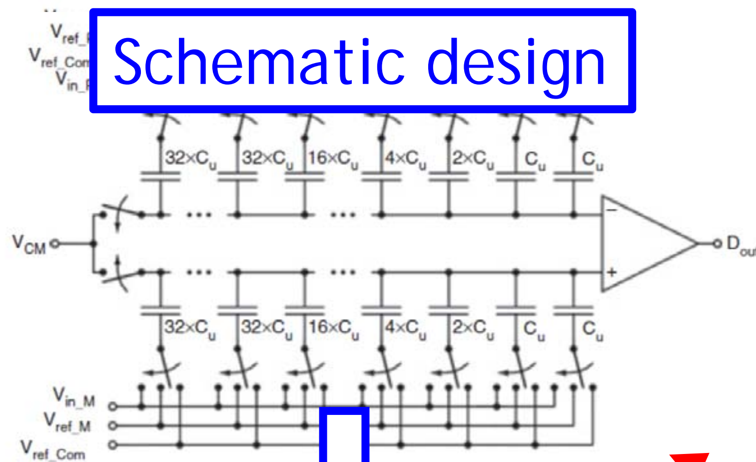
- Millions of transistors are made
- They are connected through layers of metals

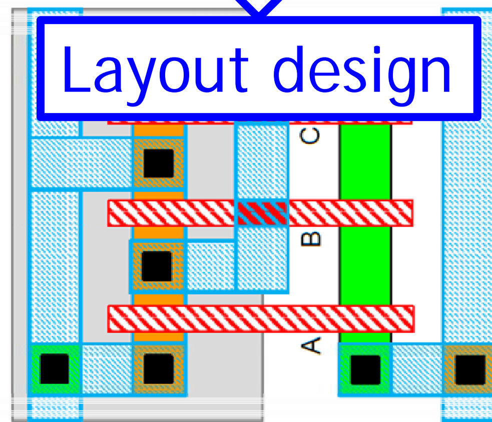


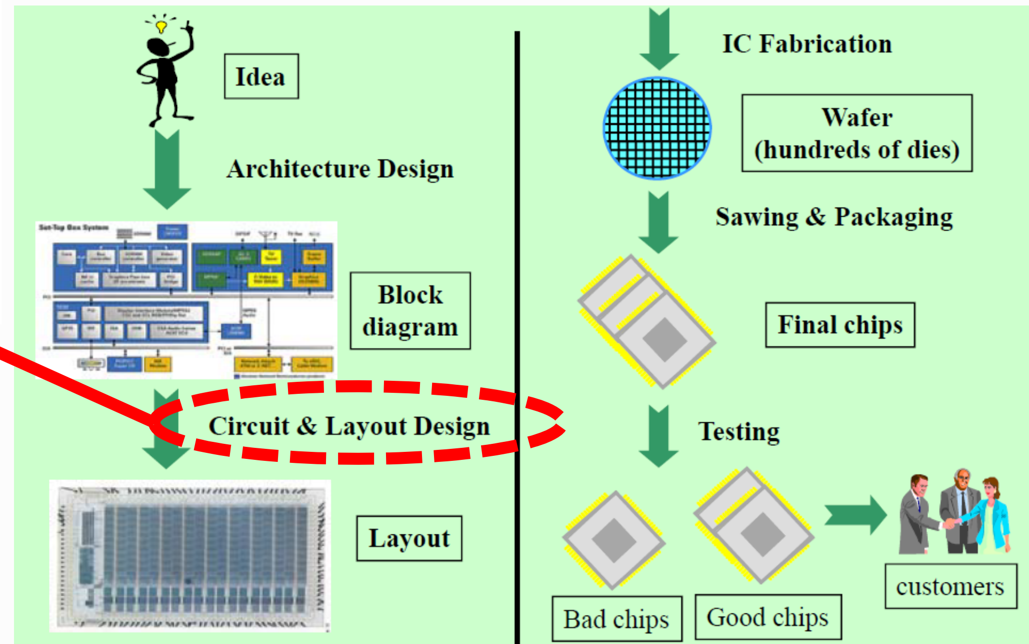


What is the role of layout

- Designer have to provide layout info. to foundry instead of schematic.



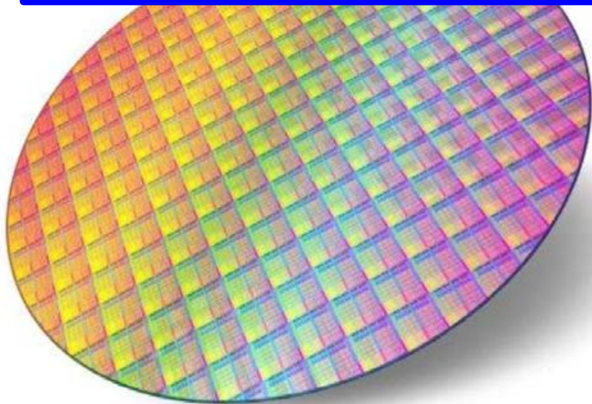




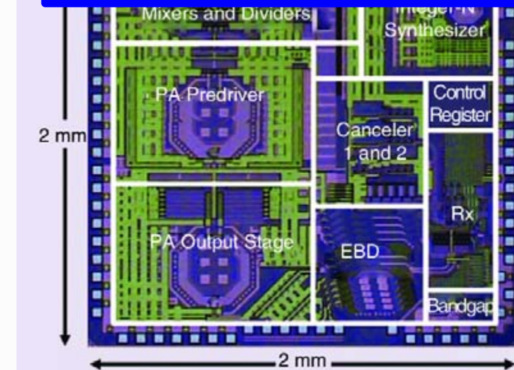
What is the role of layout

- Important role between circuit design & fabrication

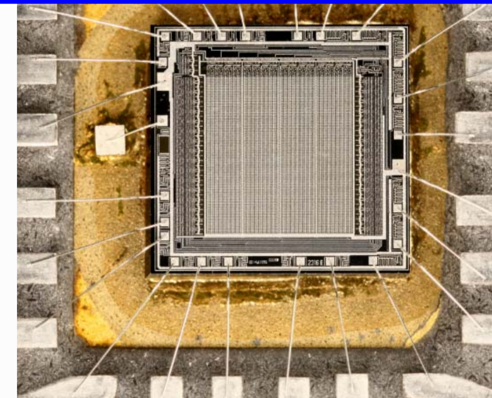
1. Fabrication (制造)



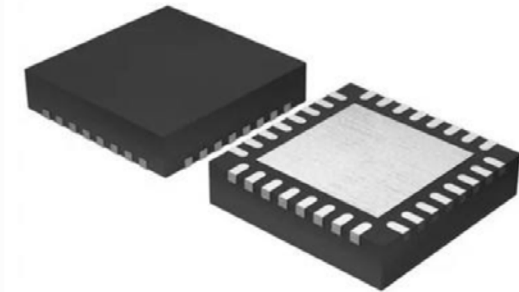
2. Dicing (划片)



3. Bonding (键合)

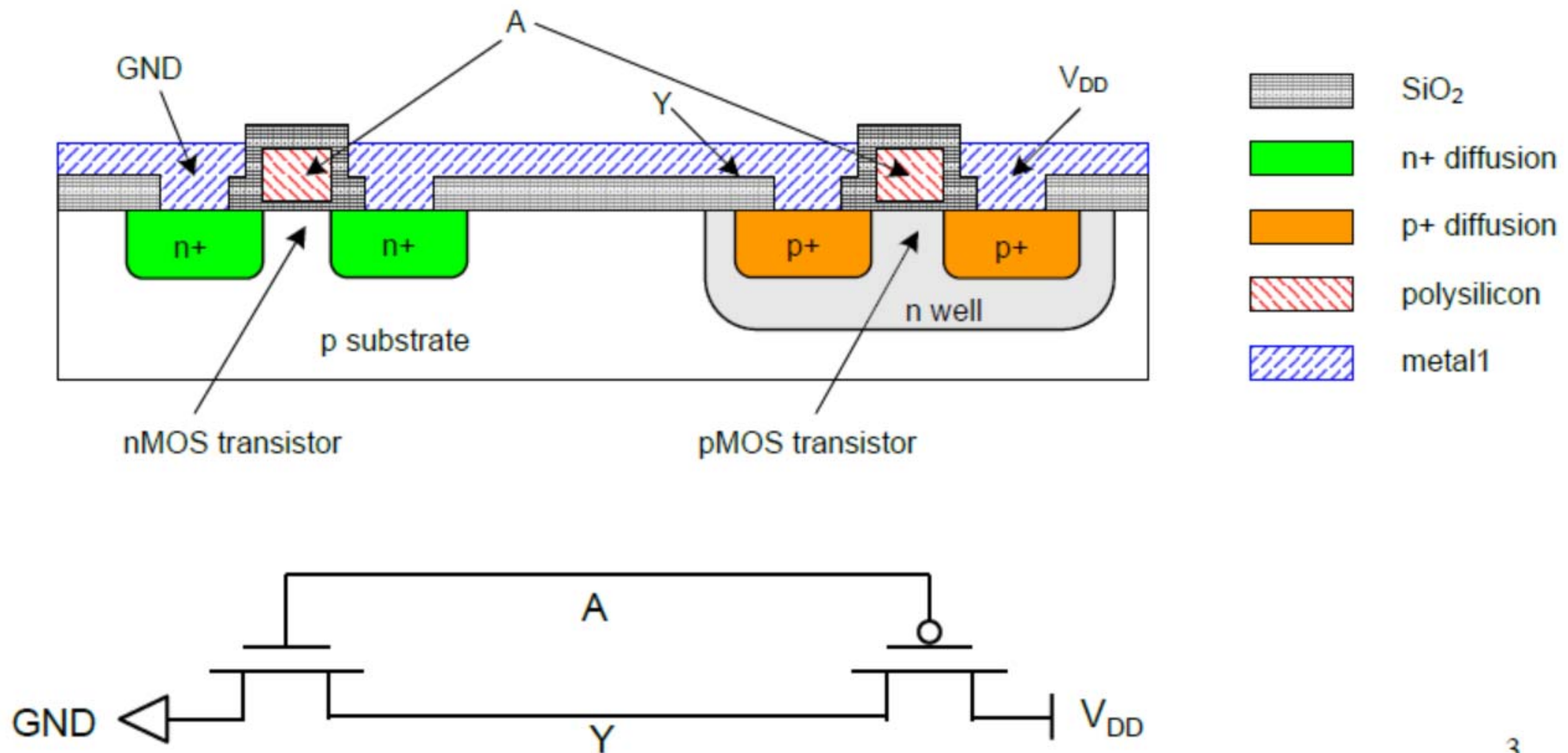


4. Packaging (封装)



What is layout?

- Layout = Manufactural design language



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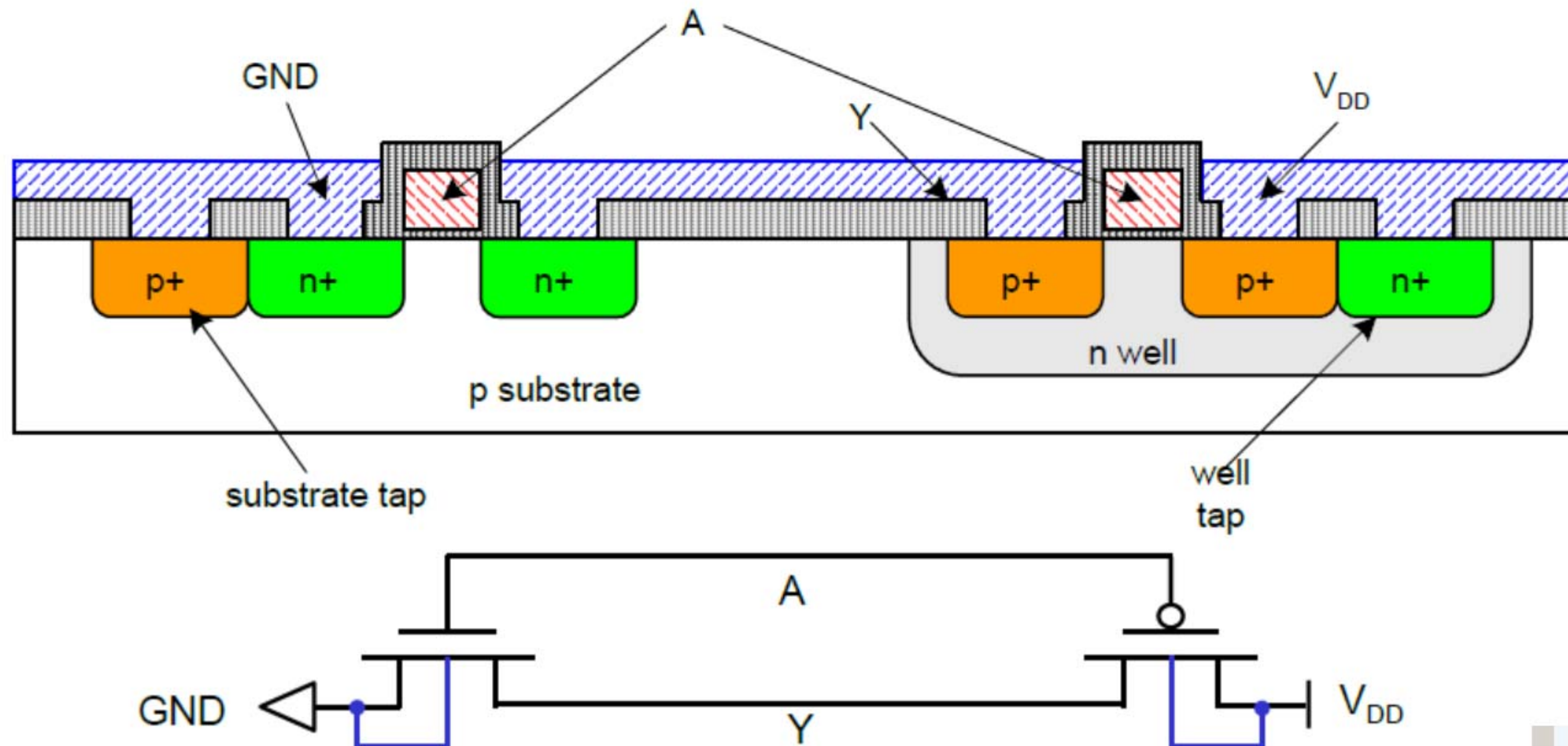
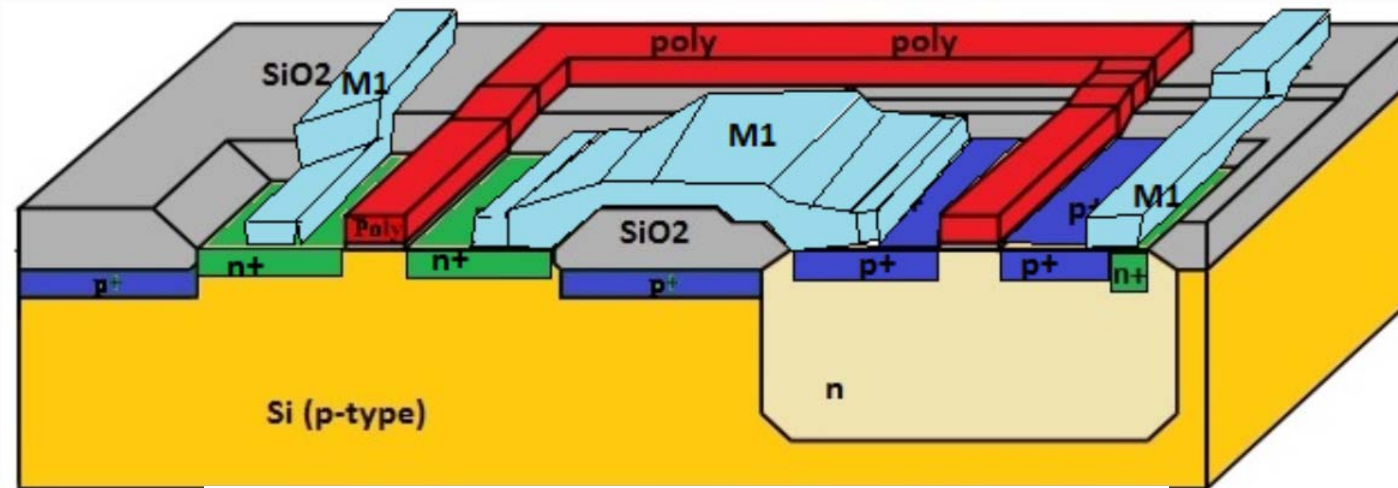
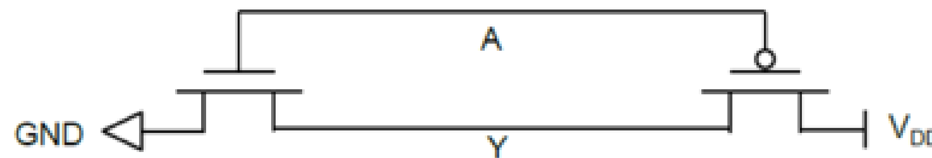


What is layout?

- A 3-D view of CMOS transistors with metals



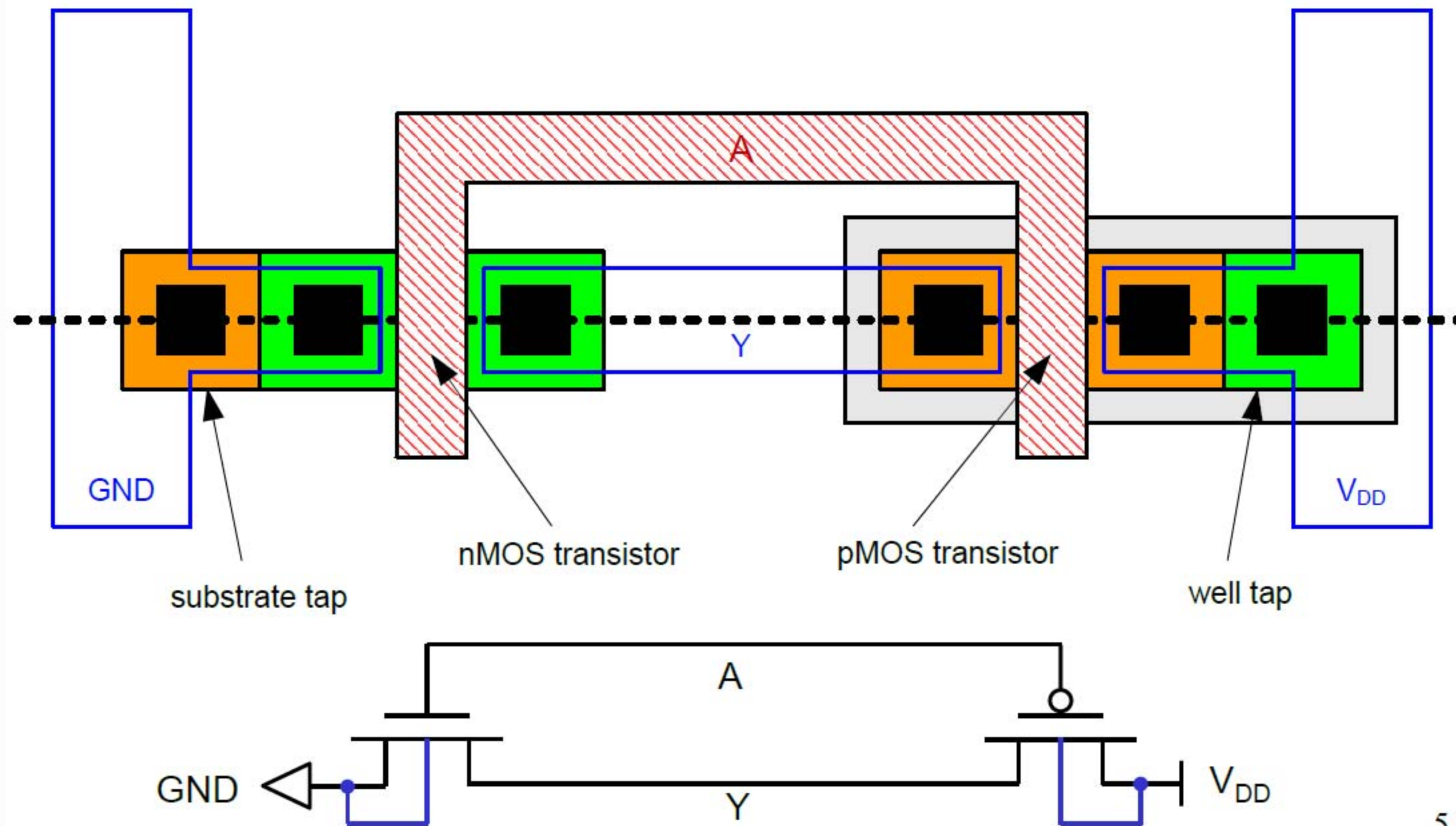


↓↓↓ Extremely clear 3-d illustration of CMOS process

http://www.vlsi-expert.com/2014/09/fabrication-steps-cmos-processing-part-1.html

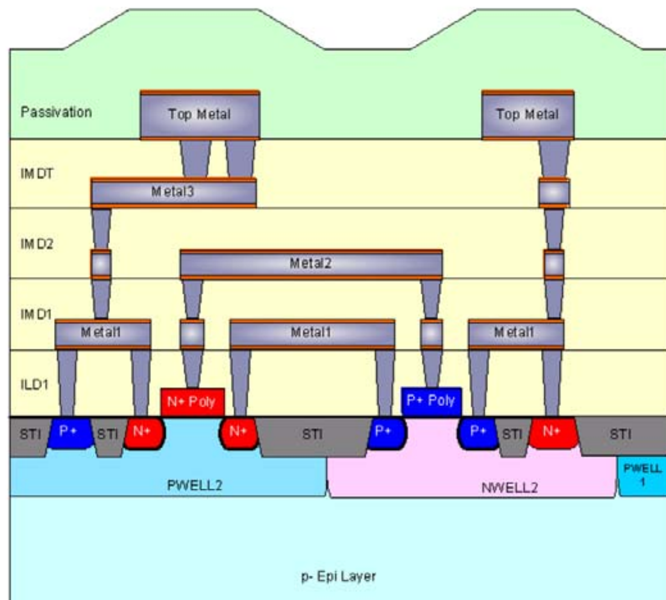
What is layout?

- Layout = Manufactural design language

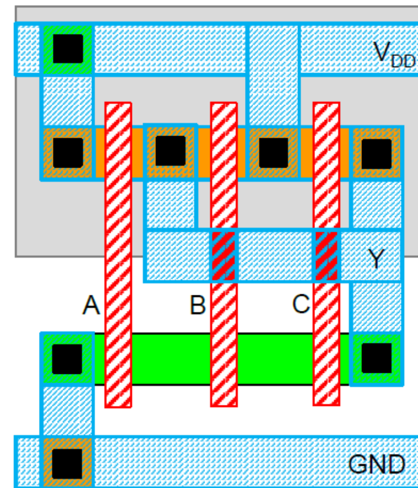


Mask to layout

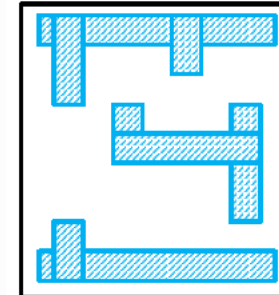
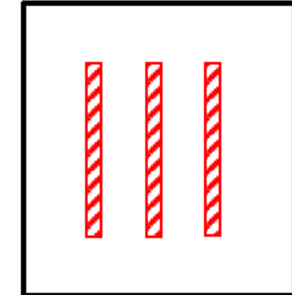
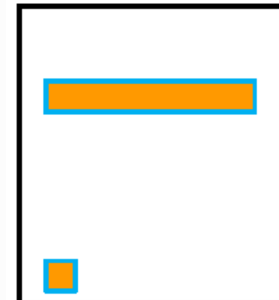
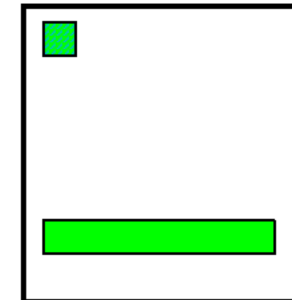
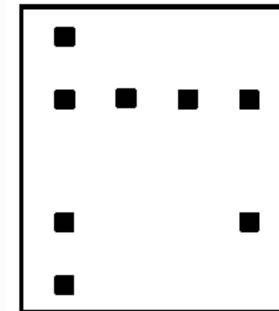
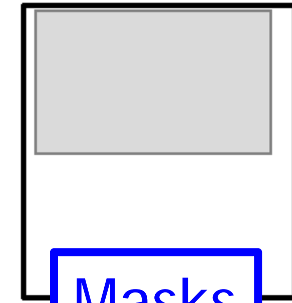
- Layout design = Mask design
- Foundry requires geometry info.



Cross-section view



Top View

Masks

Why layout is so important?

- Direct related to COST!
  - Area (cost)
  - Yield (robustness) 鲁棒性
- Imperfections (precision)
  - Process variations (matching, design rules)
  - Parasitic effects (shield, floor plan)
  - Temperature gradient (matching, floor plan)

Layout determines almost everything!
Cost, Precision, Robustness...

Why layout is so important?

- Layout is key step towards real chip
- Layout is fundamental knowledge for EDA

EDA for ADC
(模数转换器)

EDA for DAC
(数模转换器)

Outline of lecture 1 & 2

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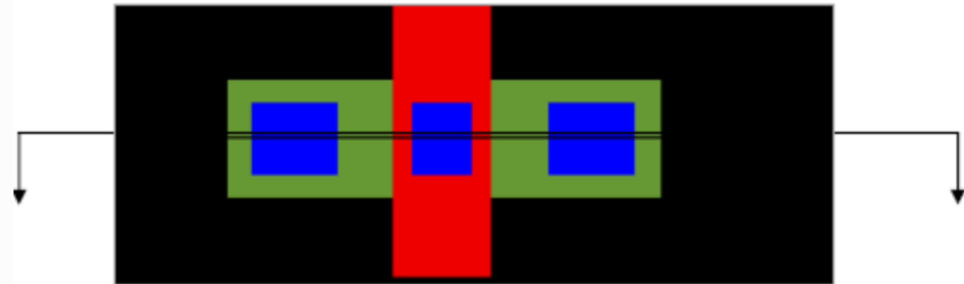
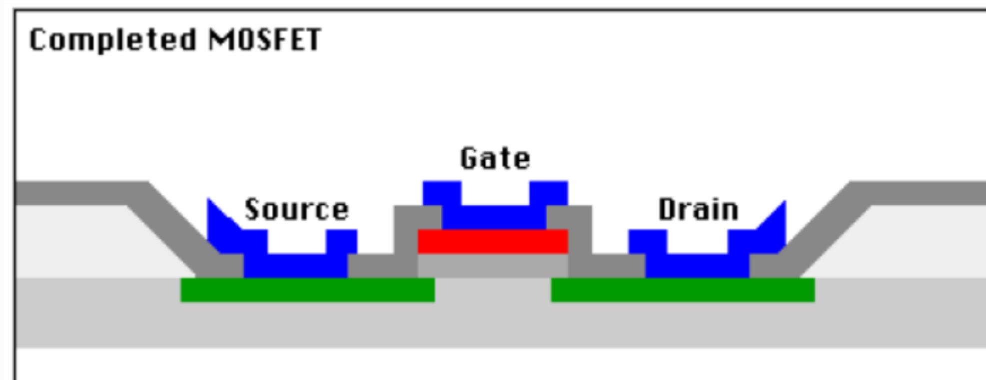
IC Fabrication Process -Example

Starting from Layout of a single NMOS

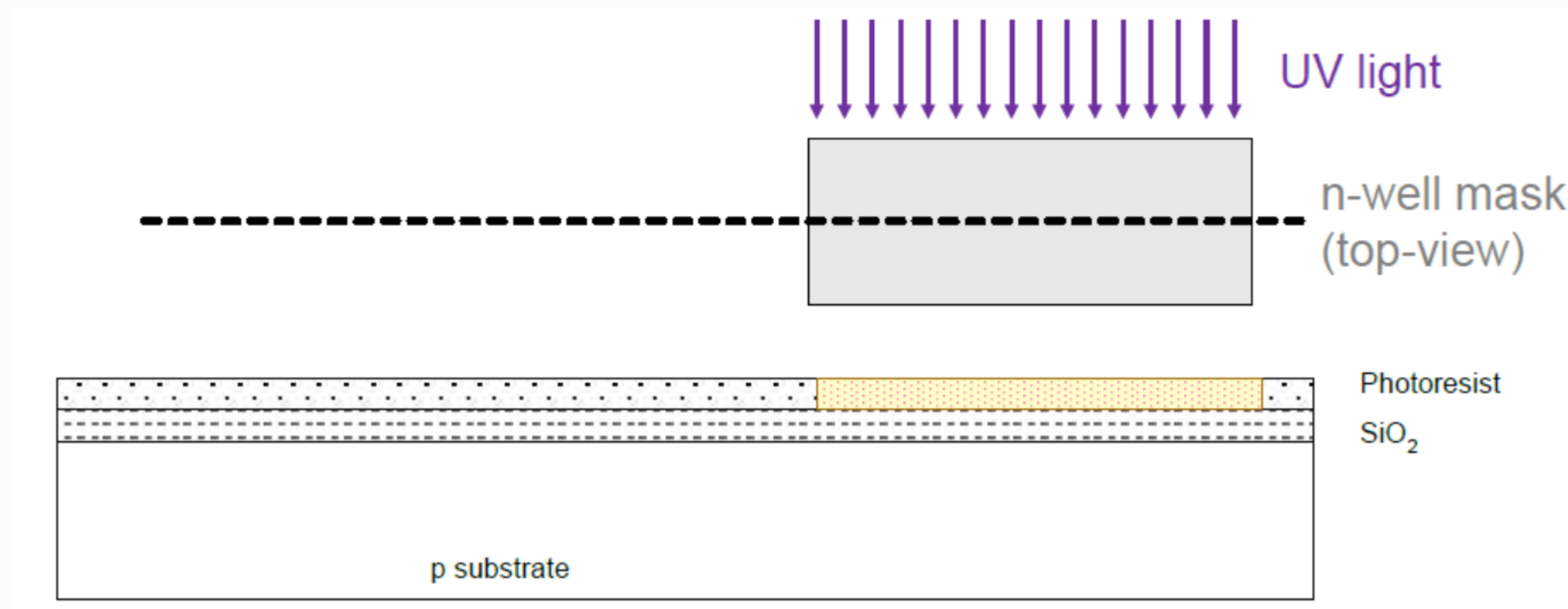


Cross-section of the finished NMOS



IC Fabrication Process –a Glance (0)

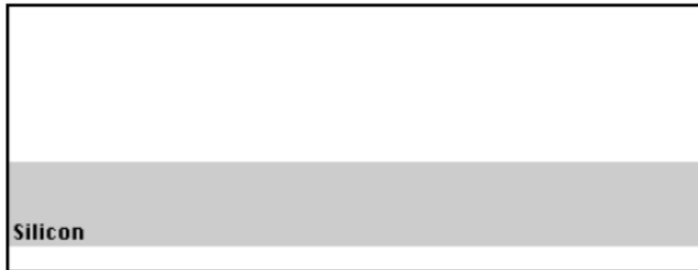
- Photoresist is a light-sensitive organic polymer
- Softens where exposed to UV light

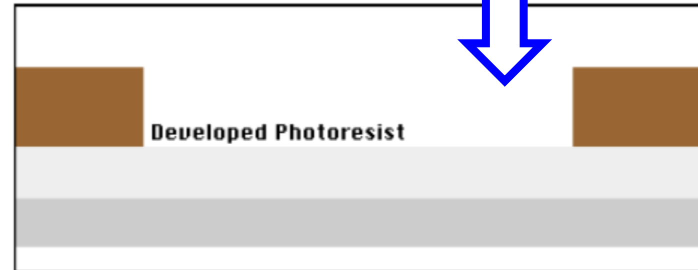


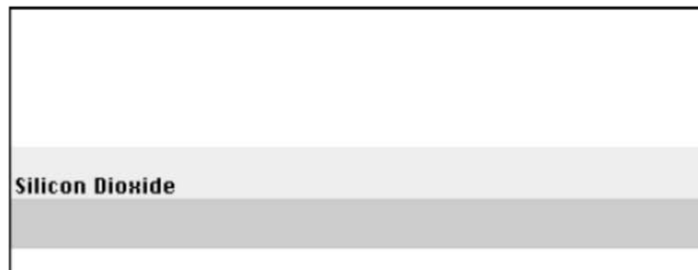
IC Fabrication Process –a Glance (1)

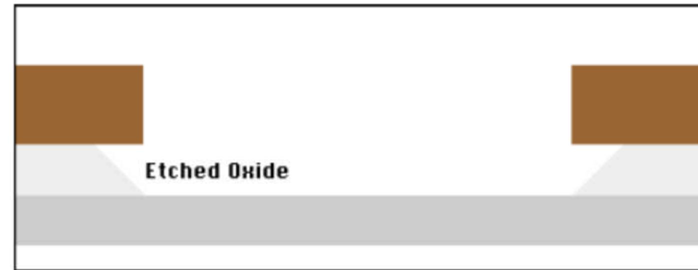
Deposition -> lithography -> etching
(沉积) (光刻) (刻蚀)

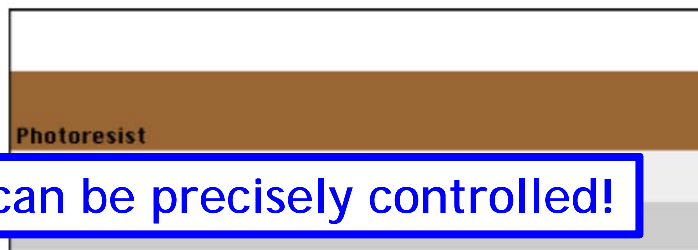
(掩模版) (图形化)
Mask & Patterning

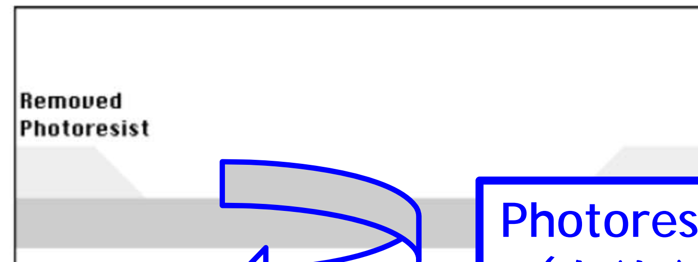










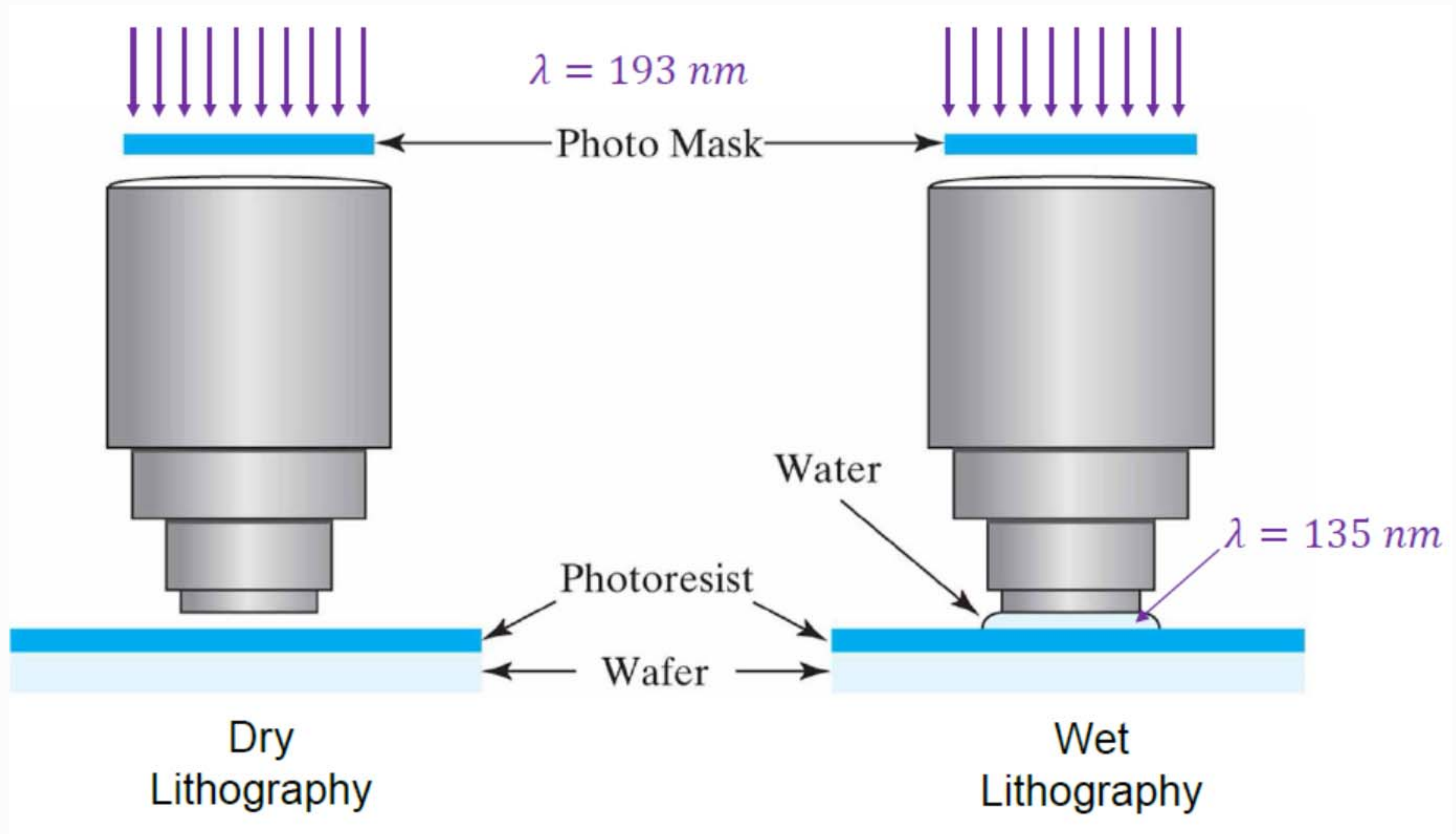


Light can be precisely controlled!

Liquid is more destructive but uncontrollable!

Photoresist
(光刻胶)

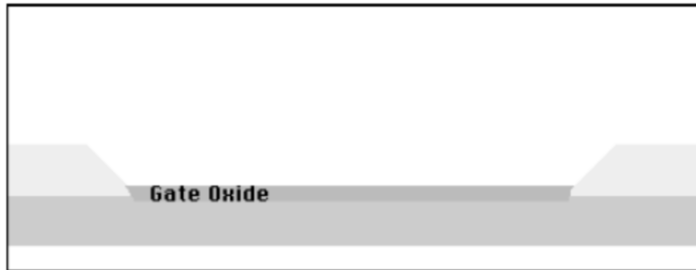
Lithography (光刻)

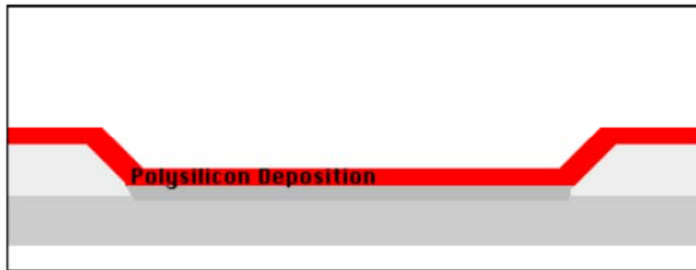


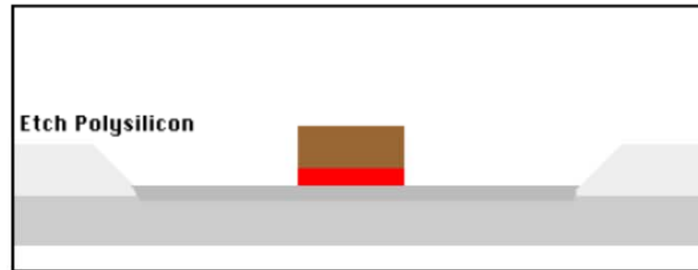
IC Fabrication Process –a Glance (2)

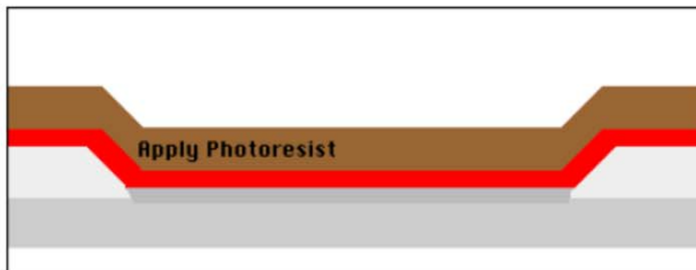
Deposition -> lithography -> etching (poly)

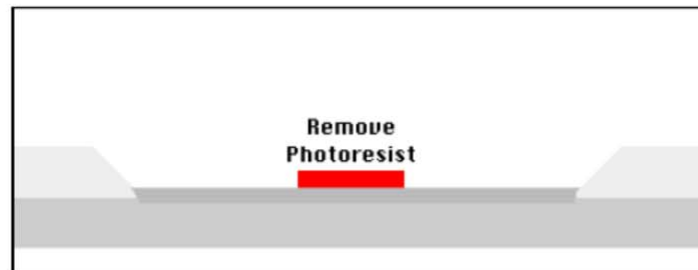
Self-aligned Tech.







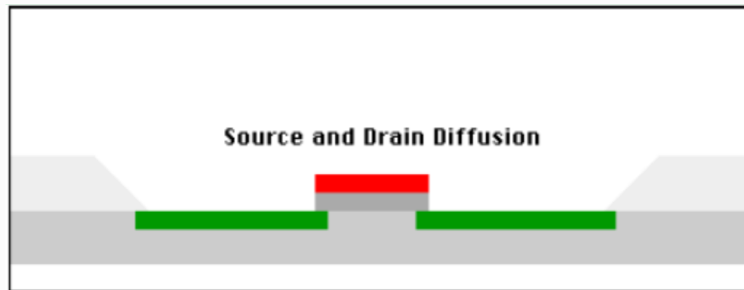


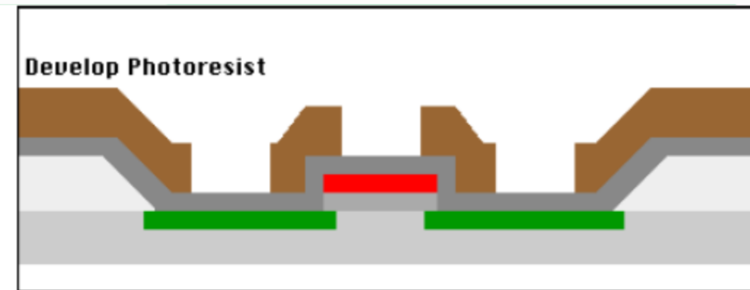


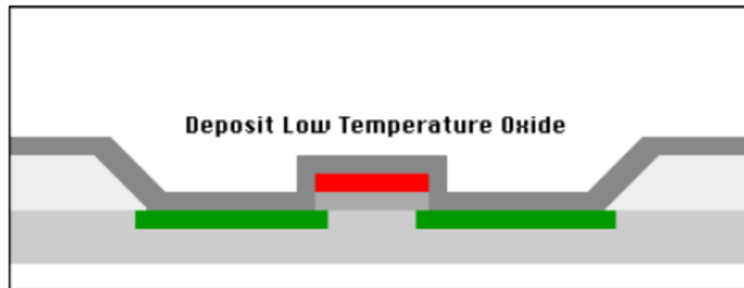
https://www.ece.ucdavis.edu/~bower/mosfetdetail.htm

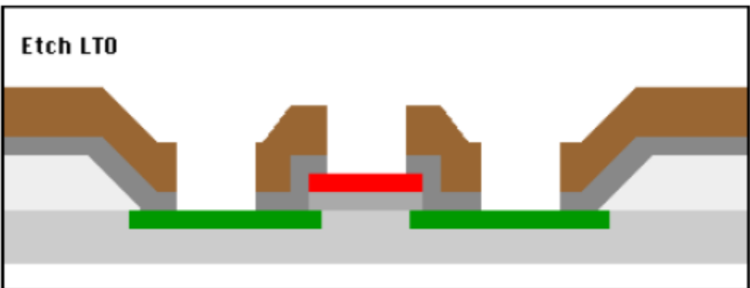
IC Fabrication Process –a Glance (3)

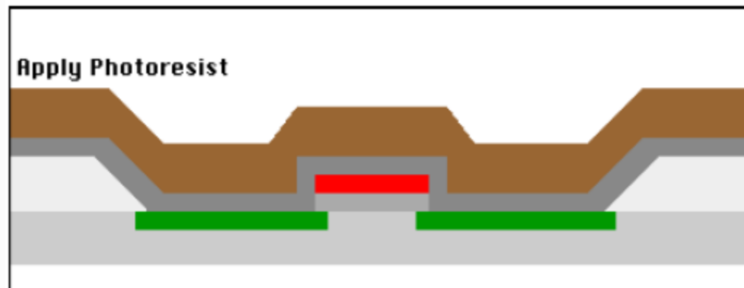
Deposition -> lithography -> etching (diffusion & oxide)

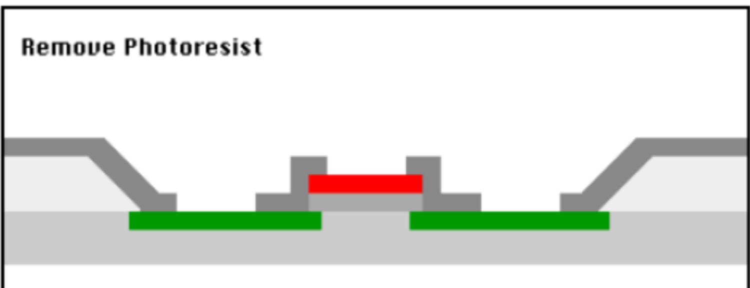






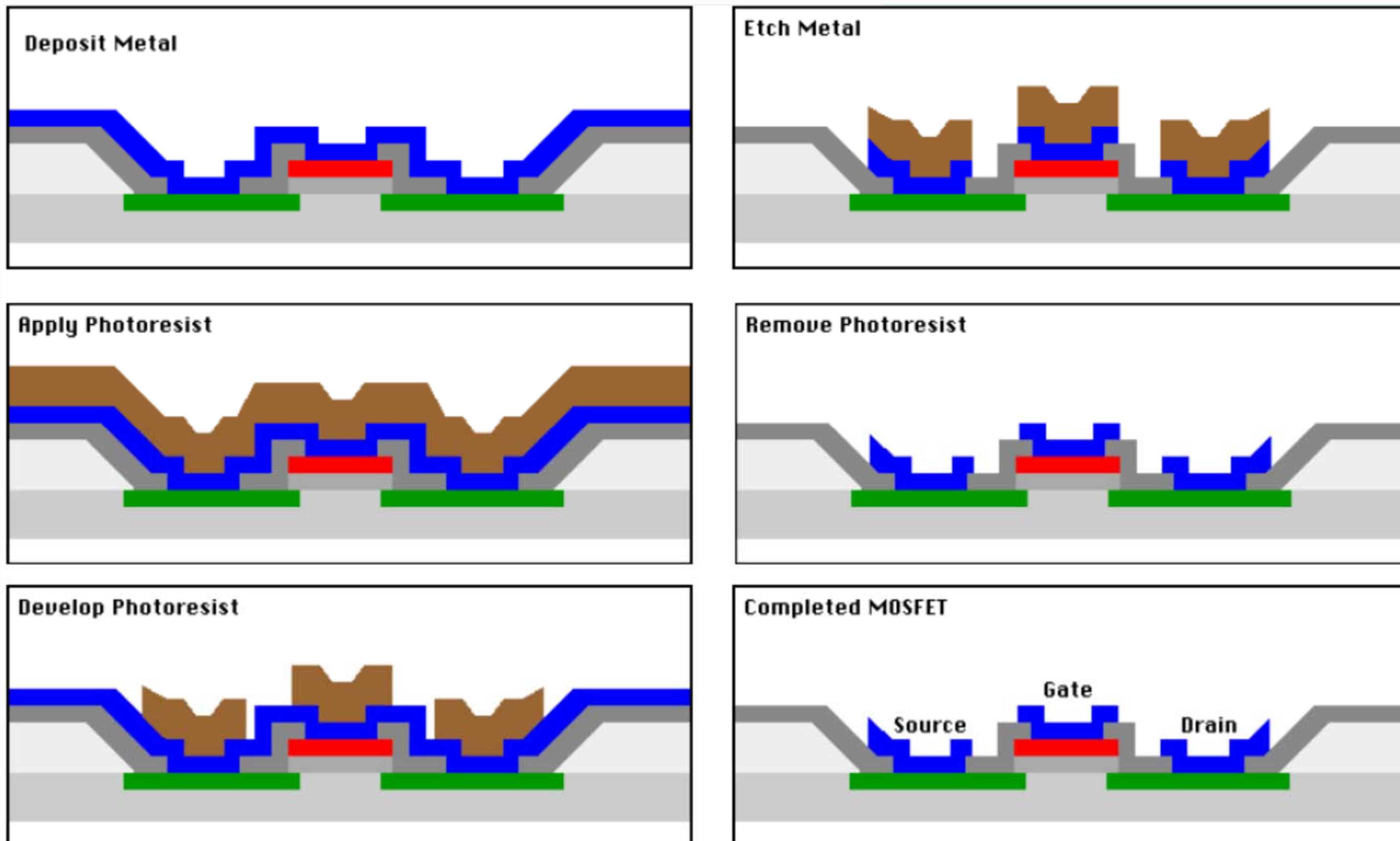






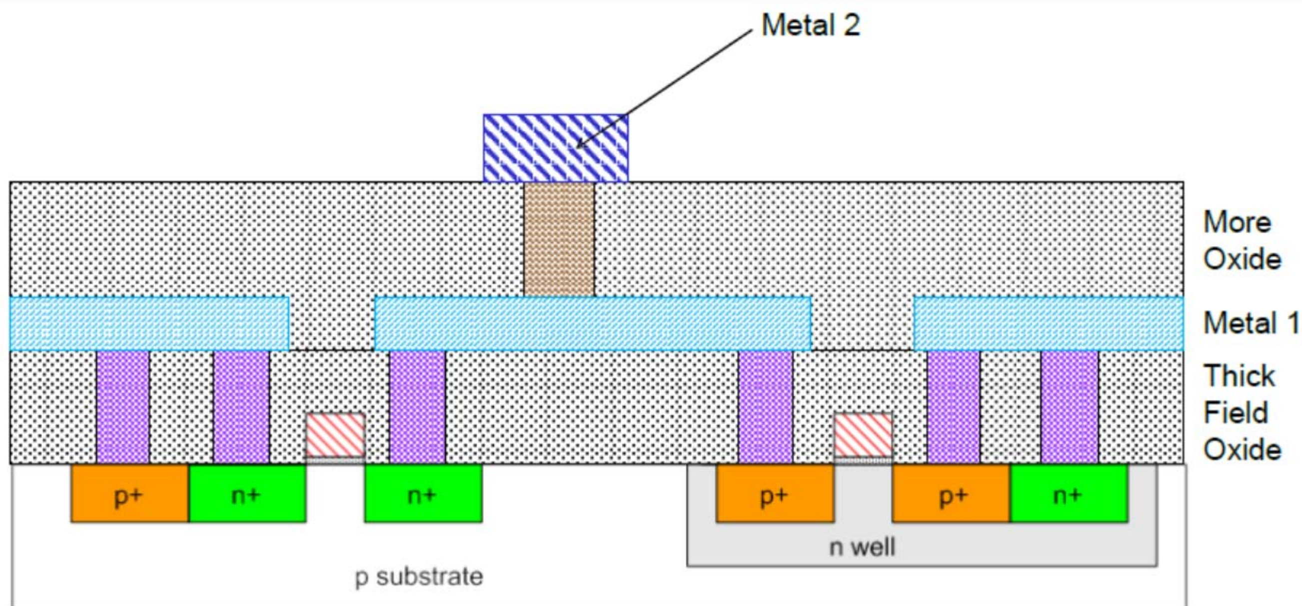
IC Fabrication Process –a Glance (4)

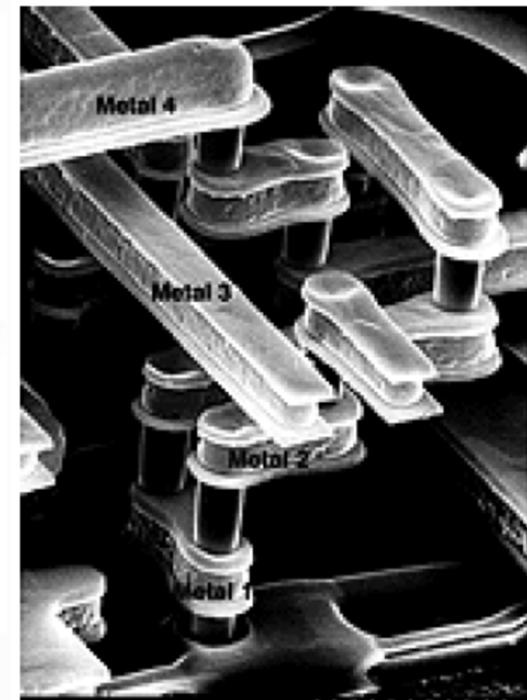
Deposition -> lithography -> etching (metal)



IC Fabrication Process –a Glance (5)

- Contact, Via and Metal are formed in the same way
  (触点) (过孔)





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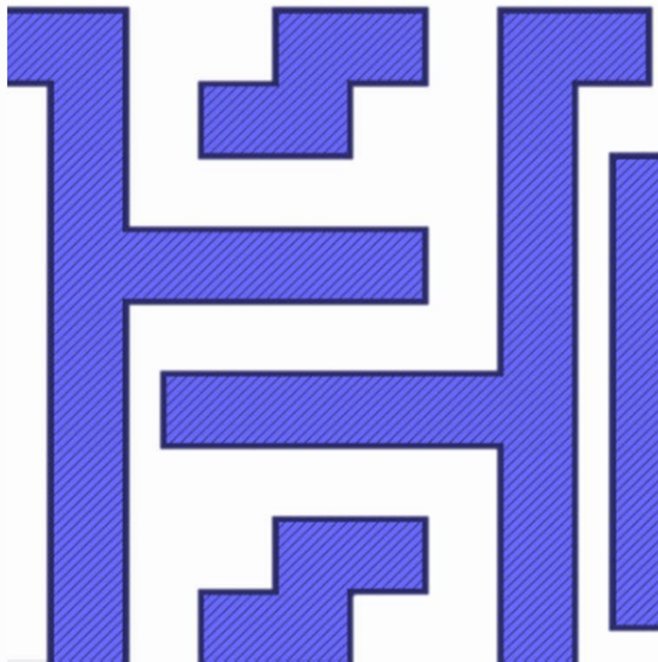
Design Rules

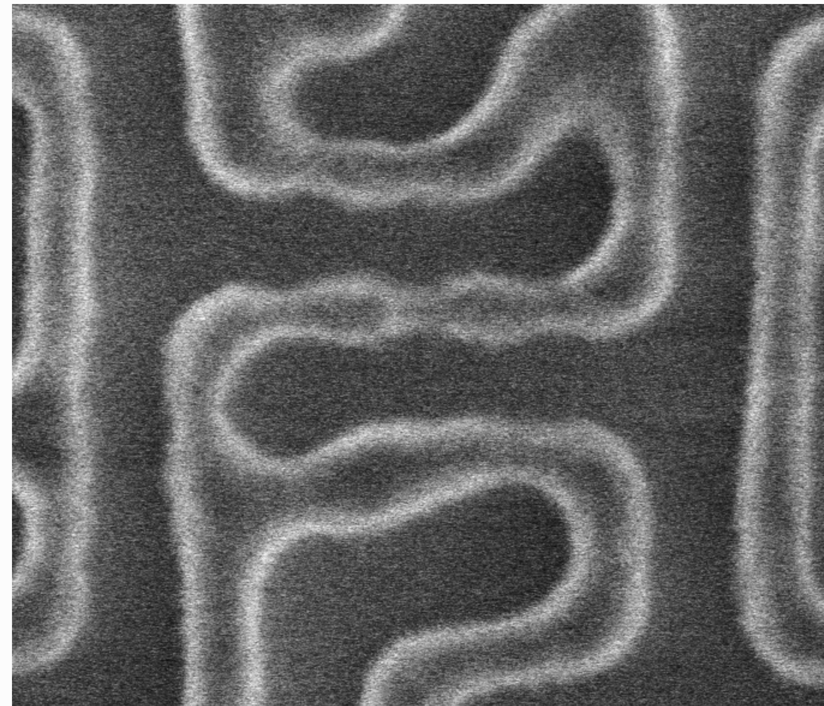
- Design rules are a set of contracts between the circuit designers and process engineers
- Four categories of Design Rules:
  - C1: Unit dimension: Minimum line width
    - Scalable design rules: lambda parameter
    - Absolute dimensions (micron rules)
  - C2: Intra-Layer rules
    - Width and spacing
  - C3: Inter-Layer rules
    - Enclosures and overlaps
  - C4: Special rules
    - Antenna rules, area, density rules

Why we need design rules?

- Defects, Impurities/dust particles
- Imperfections in photoresist / mask



Ideal case

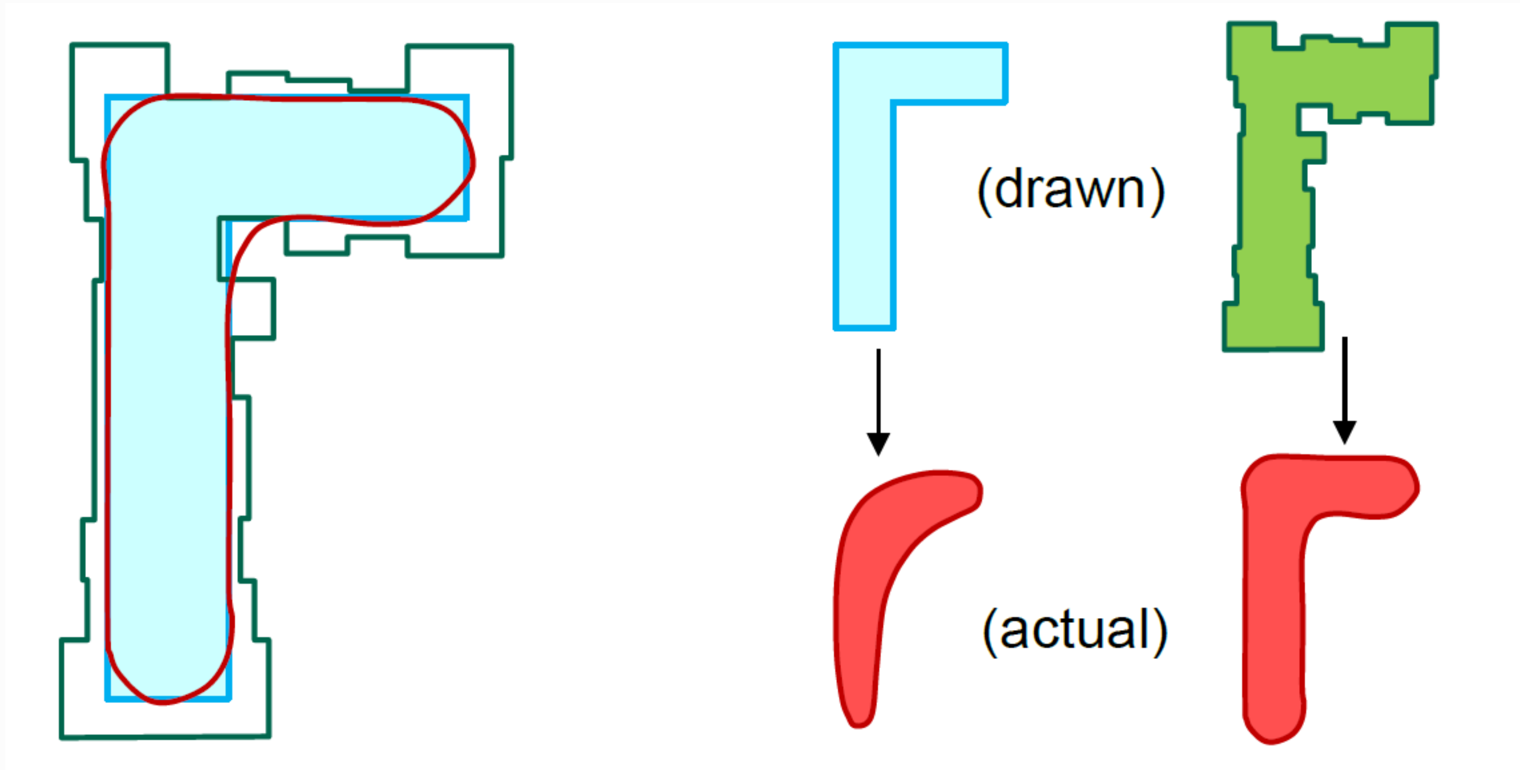


Practical case

Why we need design rules?

- Prevent mask from interference

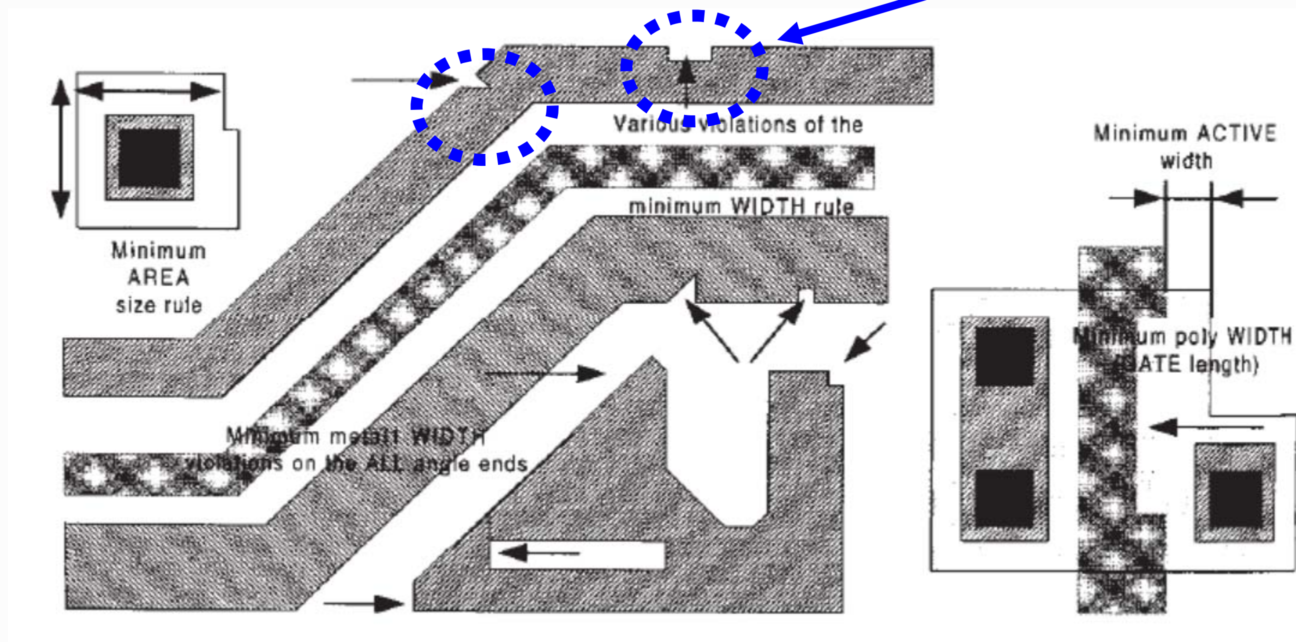
The outline of mask will be larger than the original shape!



Intra-layer rules

- Minimum width
  - Defines the resolution of technology
  - Potential open circuits or fusing
- Minimum spacing rule
  - Avoid unwanted short circuit

Process variations



Intra-layer rules

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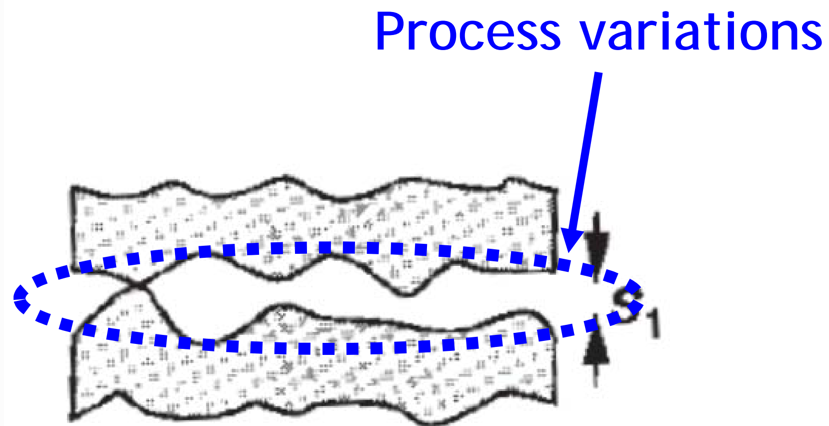
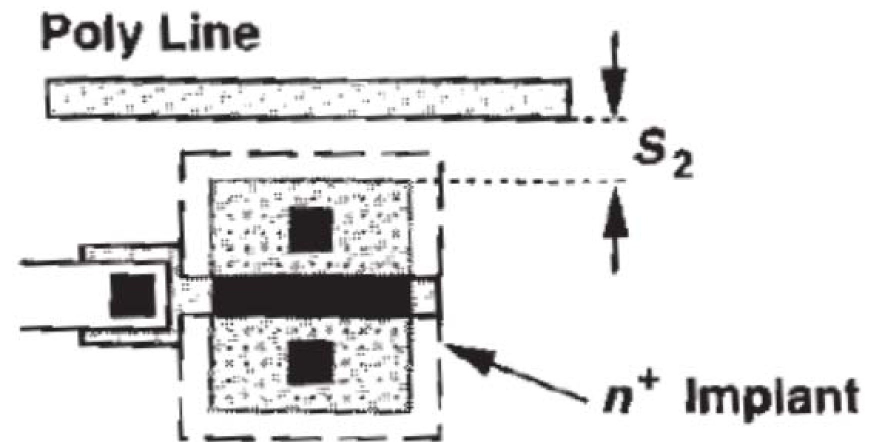
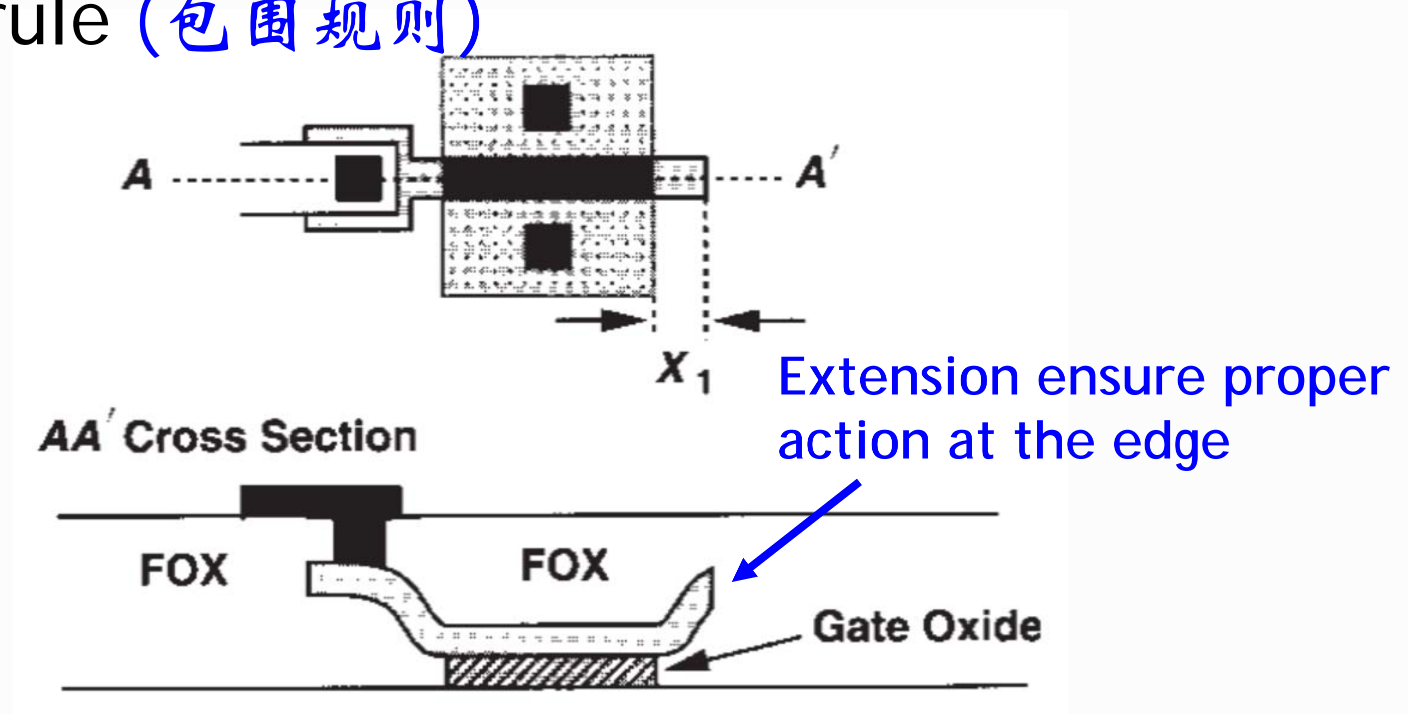




Inter-layer rules (anti-misalignment)

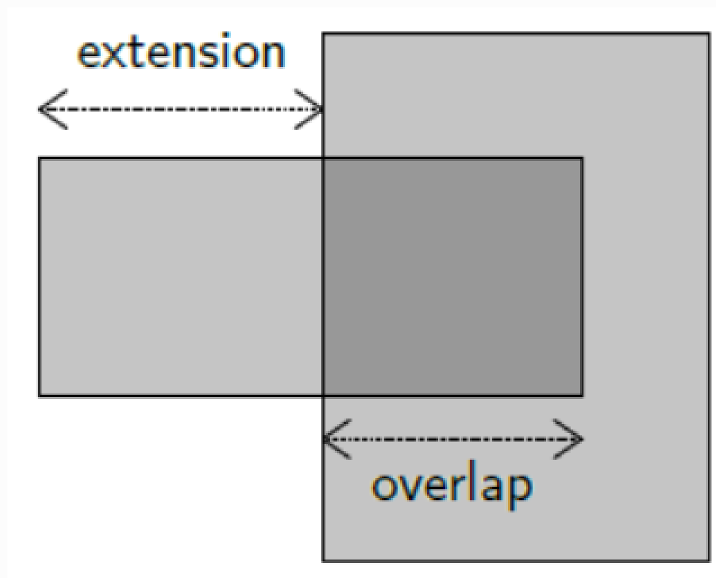
- Extension Rule (延伸规则)
  - Some geometries must extend beyond the edge of others by a minimum value
- Overlap rule (重叠规则)
- Enclosure rule (包围规则)

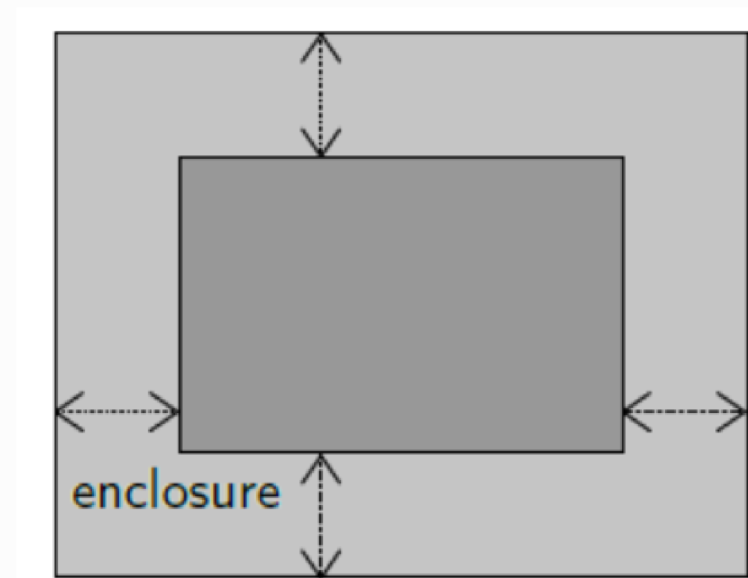


Extension ensure proper action at the edge

Inter-layer rules

- Minimum Extension Rule
- Overlap rule
- Enclosure rule
  - guarantee the contact/via area



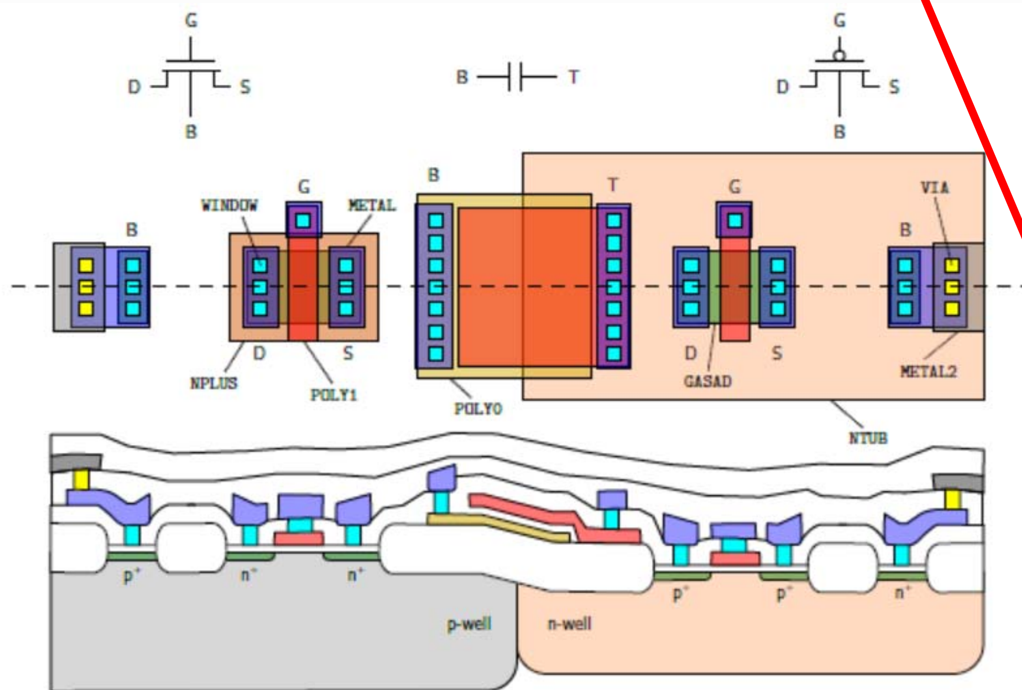


Design rules in a practical process

Poly0 width >= 2.5 μm

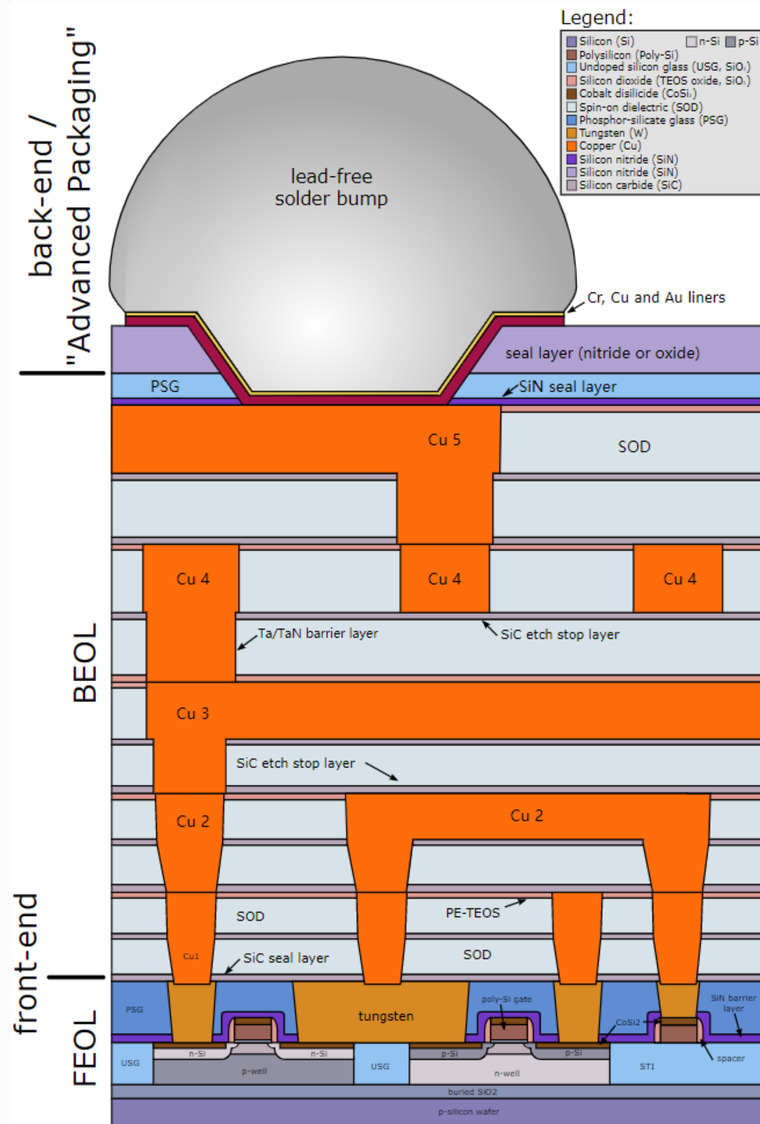
...

Poly1 enclosure of Contact >= 1.25 μm



0.0	Design grid is 0.25um x 0.25um
1.1	N-well width >= 8um
1.2	N-well spacing and notch >= 8um
2.1	GASAD width >= 2um
2.2	GASAD spacing and notch >= 4um
2.3	N-well enclosure of P-plus active >= 5um
2.4	N-well spacing to N-plus active >= 5um
3.1	Poly0 width >= 2.5um
3.2	Poly0 spacing and notch >= 6um
3.3	Poly0 spacing to GASAD >= 6um
4.1.a	Poly1 width inside GASAD >= 3um
4.1.b	Poly1 width outside GASAD >= 2.5um
4.2	Poly1 spacing and notch >= 3um
4.3	GASAD extension of Poly1 >= 3um
4.4	Poly1 extension of GASAD >= 2.5um
4.5	Poly1 spacing to GASAD >= 1.25um
4.6	Poly0 enclosure of Poly1 >= 3um
5.1	N-plus enclosure of GASAD >= 2.5um
5.2	N-plus spacing to P-plus active >= 2.5um
5.3	N-plus spacing to Poly1 inside P-plus active >= 2um
5.4	N-plus extension of Poly1 inside N-plus active >= 1.5um
5.5	N-plus width >= 2.5um
5.6	N-plus spacing and notch >= 2.5um
6.1	Exact contact size = 2.5um x 2.5um
6.2	Contact spacing >= 3um
6.3	GASAD enclosure of Contact >= 1um
6.4	Poly1 enclosure of Contact >= 1.25um
6.5	Poly1 Contact spacing to GASAD >= 2.5um
6.6	Contact spacing to Poly1 inside GASAD >= 2um
6.9	Poly0 enclosure of Contact >= 4um
6.10	Contact spacing to Poly1 & Poly0 >= 4um
7.1	Metal1 width >= 2.5um
7.2	Metal1 spacing and notch >= 3um
7.3	Metal1 enclosure of Contact >= 1.25um
8.1	Exact via size = 3um x 3um
8.2	Via spacing >= 3.5um
8.3	Metal1 enclosure of Via >= 1.25um
8.4	Via spacing to Contact >= 2.5um
8.5	Via spacing to Poly1 >= 2.5um
9.1	Metal2 width >= 3.5um
9.2	Metal2 spacing and notch >= 3.5um
9.3	Metal2 enclosure of Via >= 1.25um
10.1	Exact passivation window size = 100um x 100um

Design rules in a practical process



FEOL

BEOL

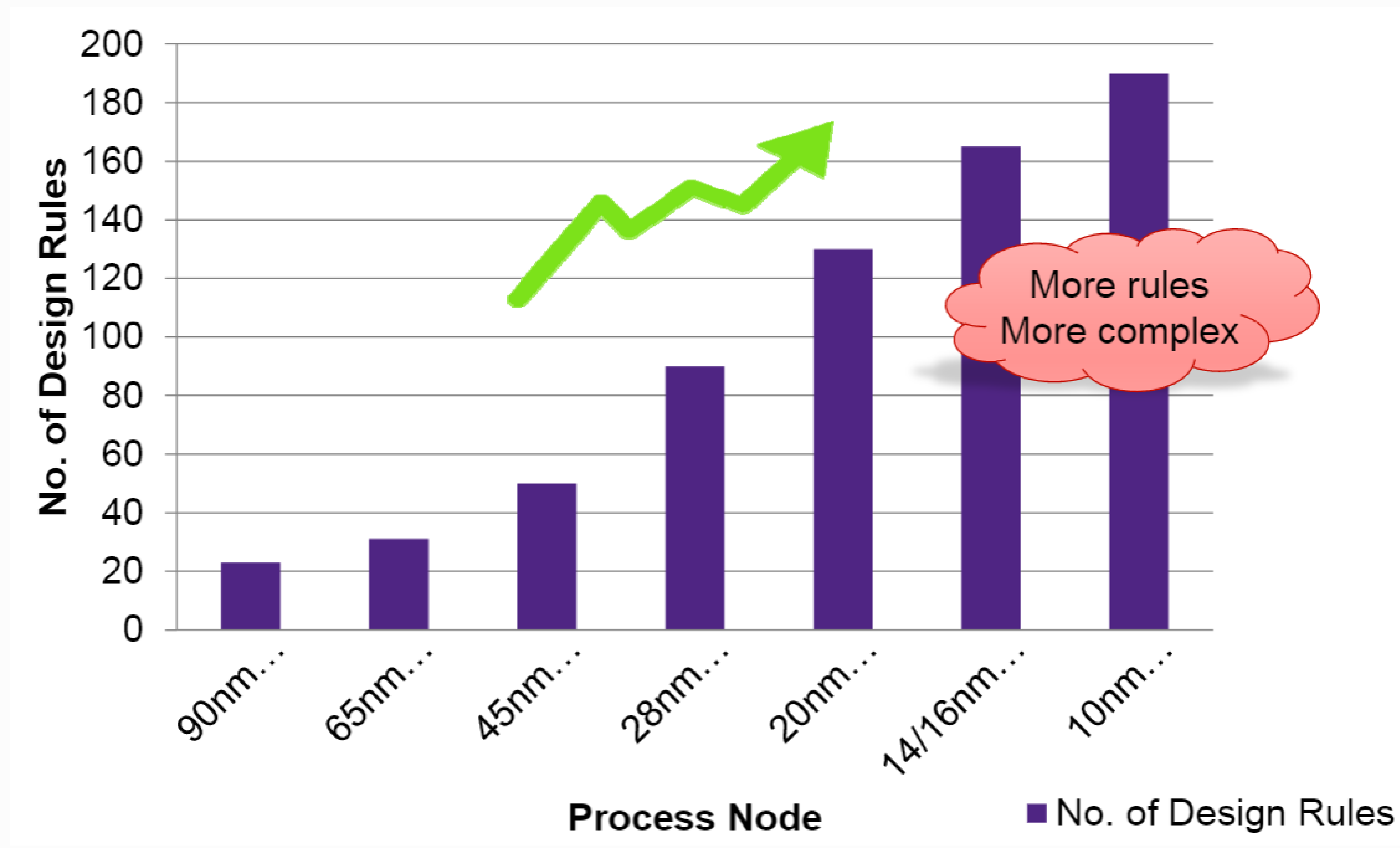
0.0	Design grid is 0.25um x 0.25um
1.1	N-well width >= 8um
1.2	N-well spacing and notch >= 8um
2.1	GASAD width >= 2um
2.2	GASAD spacing and notch >= 4um
2.3	N-well enclosure of P-plus active >= 5um
2.4	N-well spacing to N-plus active >= 5um
3.1	Pol
3.2	Pol
3.3	Pol
4.1.a	Pol
4.1.b	Pol
4.2	Pol
4.3	GASAD extension of Poly1 >= 3um
4.4	Poly1 extension of GASAD >= 2.5um
4.5	Poly1 spacing to GASAD >= 1.25um
4.6	Poly0 enclosure of Poly1 >= 3um
5.1	N-plus enclosure of GASAD >= 2.5um
5.2	N-plus spacing to P-plus active >= 2.5um
5.3	N-plus spacing to Poly1 inside P-plus active >= 2um
5.4	N-plus extension of Poly1 inside N-plus active >= 1.5um
5.5	N-plus width >= 2.5um
5.6	N-plus spacing and notch >= 2.5um
6.1	Exact contact size = 2.5um x 2.5um
6.2	Contact spacing >= 3um
6.3	GASAD enclosure of Contact >= 1um
6.4	Poly1 enclosure of Contact >= 1.25um
6.5	Poly1 Contact spacing to GASAD >= 2.5um
6.6	Contact spacing to Poly1 inside GASAD >= 2um
6.9	Poly0 enclosure of Contact >= 4um
6.10	Contact spacing to Poly1 & Poly0 >= 4um
7.1	Metal1 width >= 2.5um
7.2	Me
7.3	Me
8.1	Ex
8.2	Vi
8.3	Me
8.4	Vi
8.5	Via spacing to Poly1 >= 2.5um
9.1	Metal2 width >= 3.5um
9.2	Metal2 spacing and notch >= 3.5um
9.3	Metal2 enclosure of Via >= 1.25um
10.1	Exact passivation window size = 100um x 100um

Front-end of line
前端工艺

Back-end of line
后端工艺

Complexity of the design rules

- More design rules refer to the process document.



Outline of lecture 1 & 2

- Introduction of Analog Layout
- CMOS process brief
- Design rules
- Basic cells layout
- Design flow of Analog layout (DRC, LVS, PEX)

Layout of Basic Cells

- Layout of Transistors
- Layout of Resistors
  - Categories of resistors
  - Layout of resistors
- Layout of Capacitors
  - Categories of resistors
  - Layout of resistors

Layout of transistors

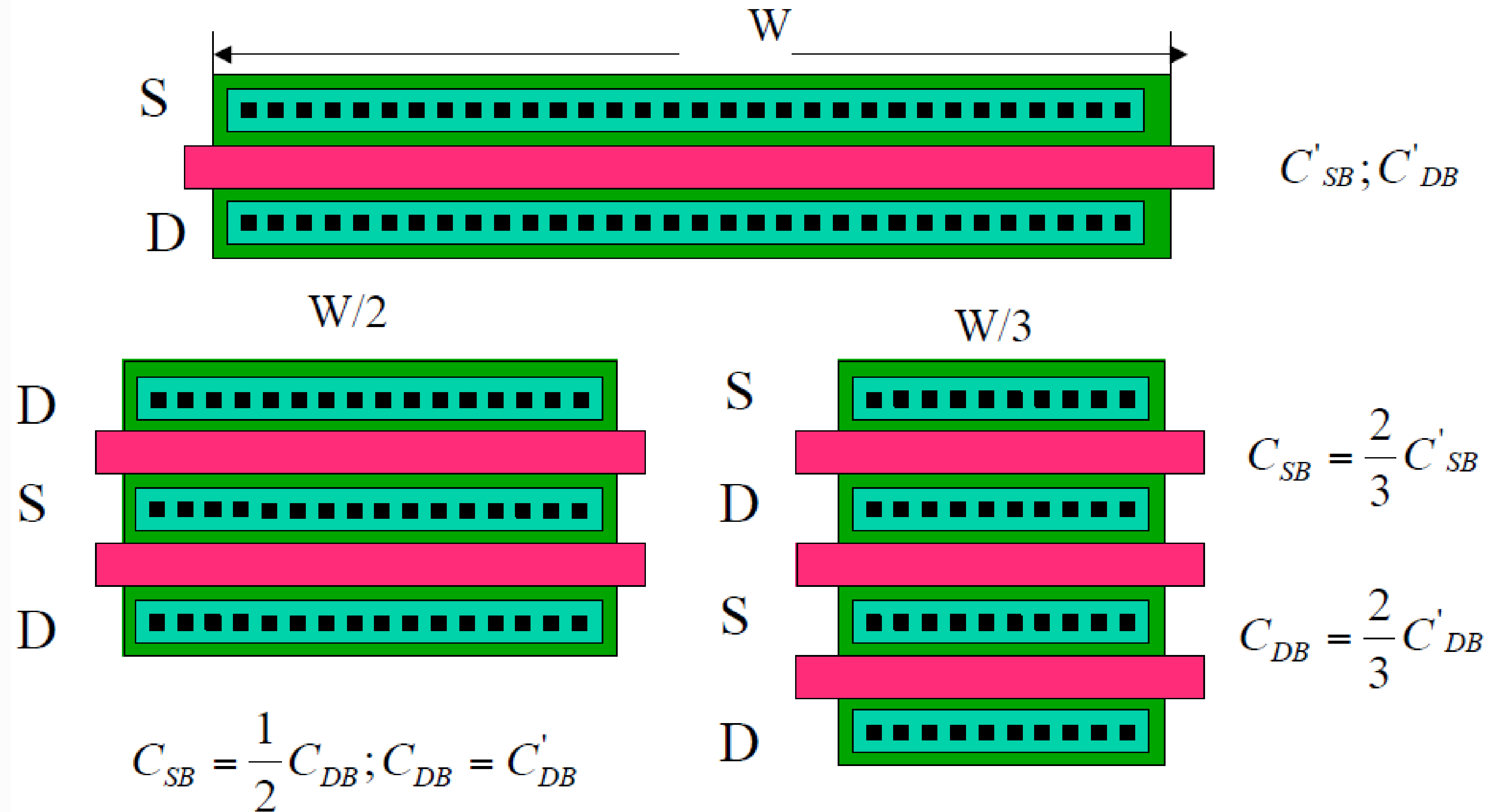
- Parasitic parameters in transistors w./ large W/L

- Large area leads to large parasitic

Process dependent! Gain, GBW...

Layout of transistors

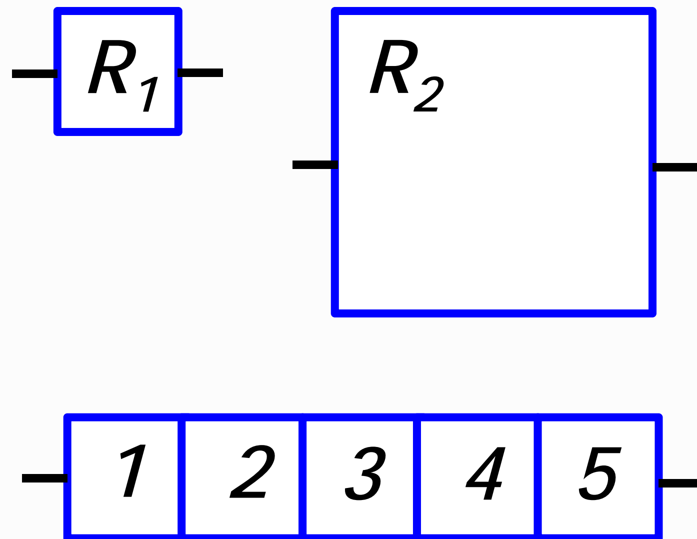
- Multi-finger approaches to reduce parasitic para.

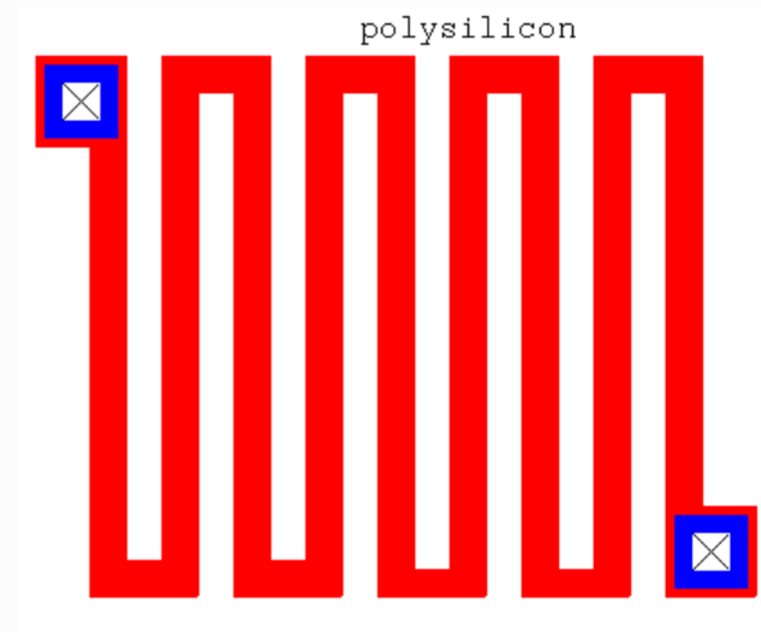


How to reduce parasitic cap under same process?

Concept of CMOS Resistors

- Which shape has larger resistance?
- Unit of CMOS resistor: Ohm/square or Ohm/□



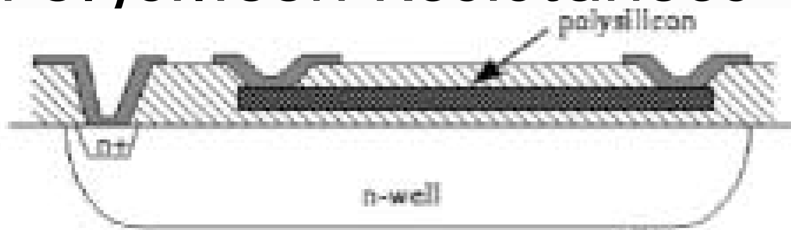


$$R = L/W * R_{square} = N_{square} * R_{square}$$

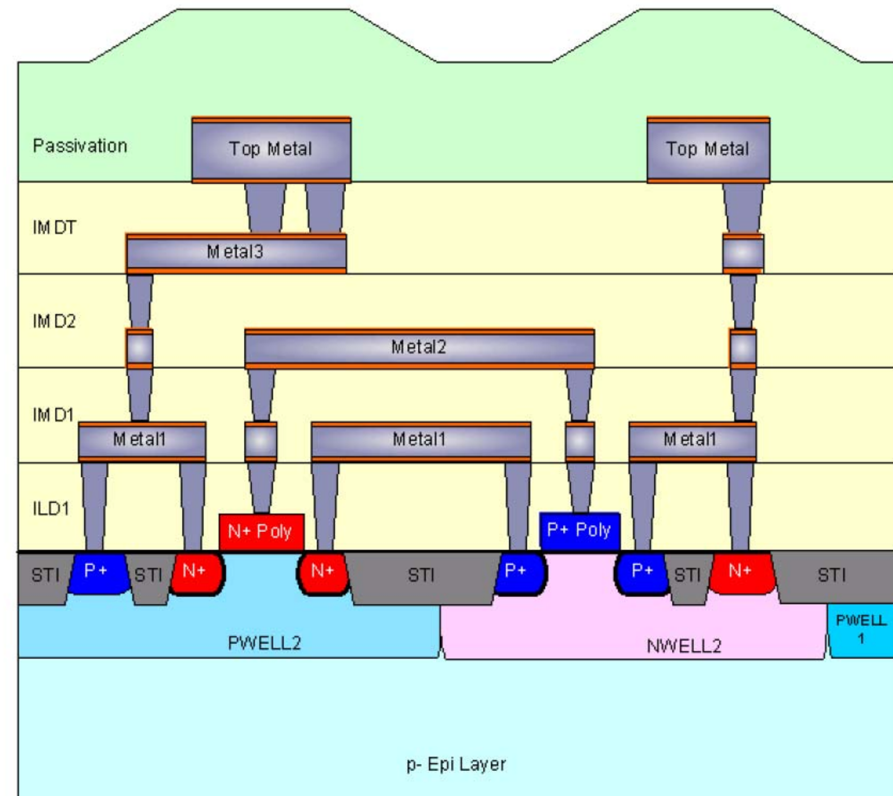
Categories of Resistors

- Diffused Resistances
  - diffused area, p^+, p^-, n^+, n^-

- Polysilicon Resistances



- Well Resistances



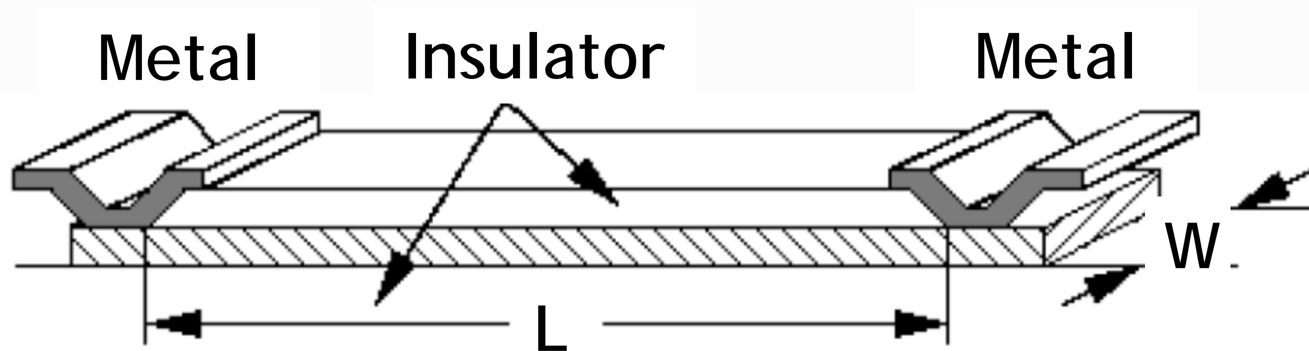
Layout of resistors

- Accuracy of Resistors
  - Suffer from process, temperature & voltage variation

Type of layer	Sheet Resistance Ω/0	Accuracy %	Temperature Coefficient ppm/°C	Voltage Coefficient ppm/V
n + diff	30 - 50	20 - 40	200 - 1K	50 - 300
p + diff	50 -150	20 - 40	200 - 1K	50 - 300
n - well	2K - 4K	15 - 30	5K	10K
p - well	3K - 6K	15 - 30	5K	10K
pinched n - well	6K - 10K	25 - 40	10K	20K
pinched p - well	9K - 13K	25 - 40	10K	20K
first poly	20 - 40	25 - 40	500 - 1500	20 - 200
second poly	15 - 40	25 - 40	500 - 1500	20 - 200

Intrinsic errors of CMOS resistors

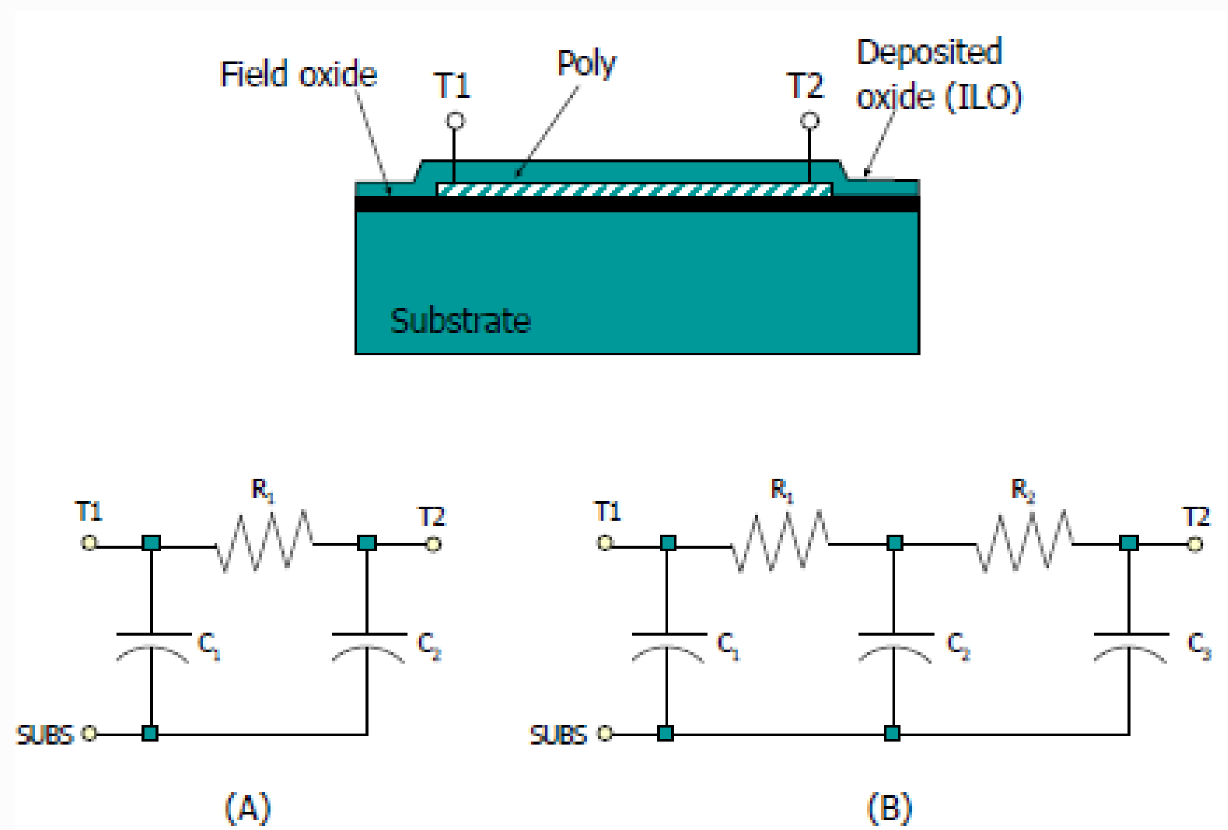
- Contact resistance
- Parasitic capacitors in CMOS resistor



$$R = 2R_{cont} + \frac{L}{W}R_{\square}$$

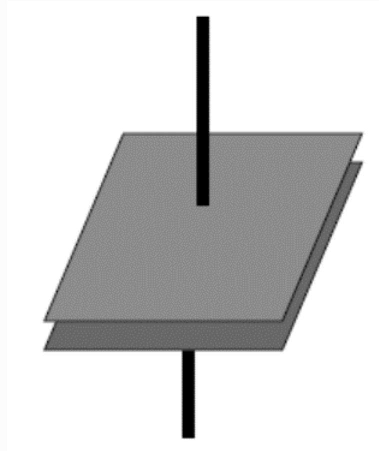
Intrinsic errors of CMOS resistors

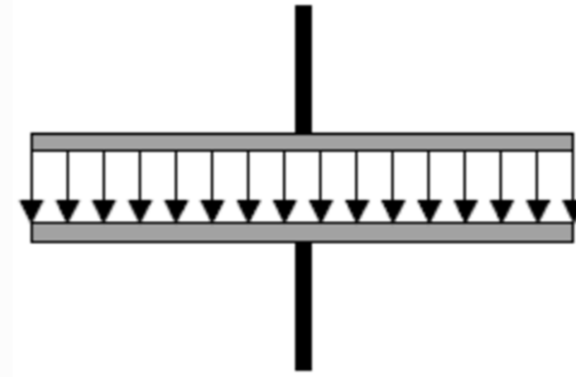
- Contact resistance
- Parasitic capacitors in CMOS resistor



What is Capacitors

Model for capacitors.





$$C = \varepsilon_O \varepsilon_r \, WL/t_{ox}$$

ε_r: relative permittivity

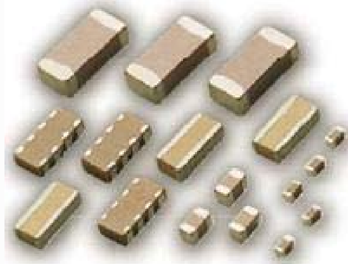
WL: area of overlapping region

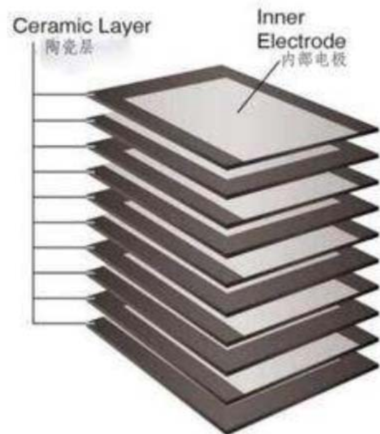
t_{ox}: thickness of overlapping region

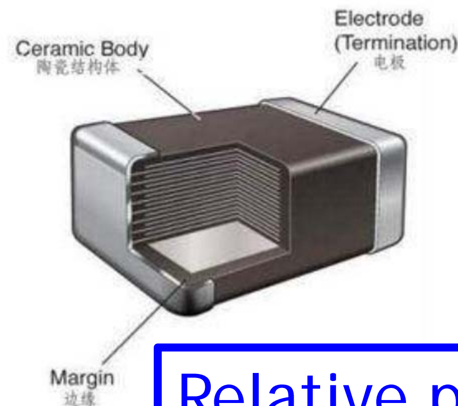
Non-CMOS (discrete) capacitors

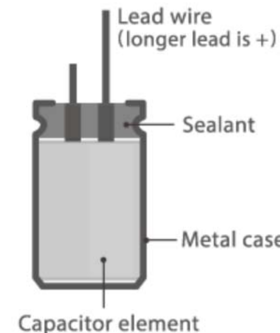
- Multi-layer ceramic cap (陶瓷电容)
- Electrolytic capacitor (电解电容)

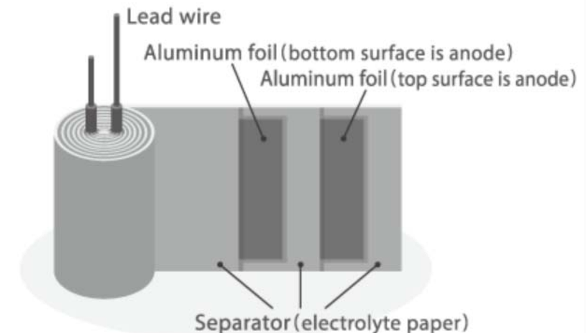
$$C = \varepsilon_O \varepsilon_r WL/t_{ox}$$











Relative permittivity 10~100

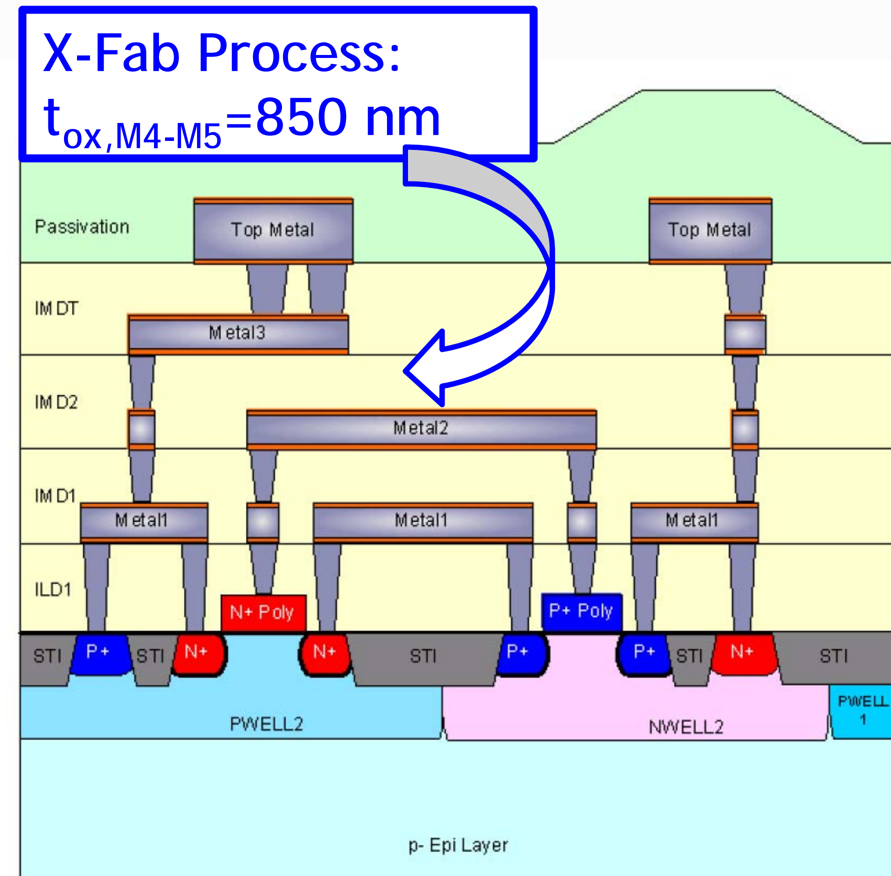
Typical value: 1pF (10^{-12}) ~ 100 μF (10^{-4})!!!

CMOS capacitors

- Drawbacks
  - Low permittivity
  - Limited stack layers (<3)
  - Extra-tech to reduce t_{ox}

$$C = \varepsilon_O \varepsilon_r WL/t_{ox}$$

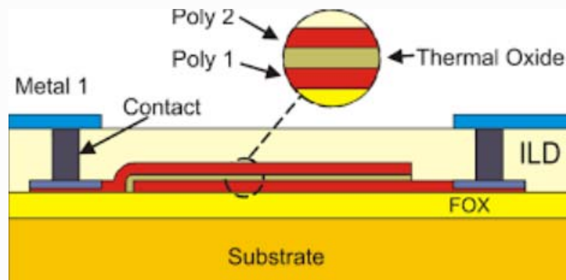
X-Fab Process:
$t_{ox,M4\text{-}M5}$=850 nm



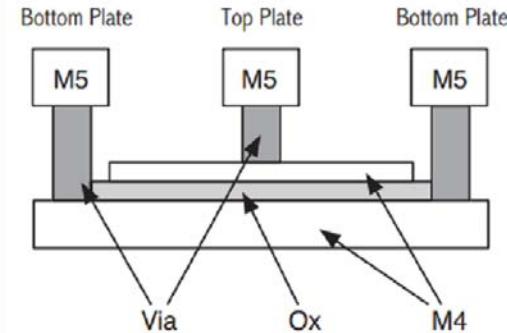
Material	Rel. Permittivity
SiO_2 Dry Oxide	3.9
SiO_2 Plasma	4.9
Si_3N_4 LPCVD	6-7
Si_3N_4 Plasma	6-9

Different categories of Cap.

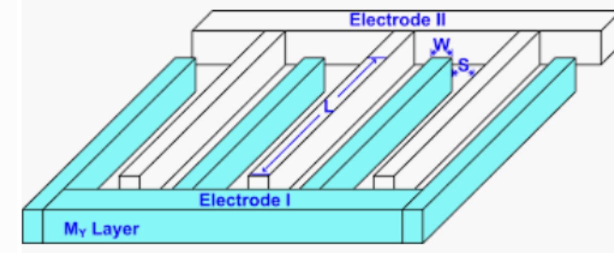
- How to form a parallel plate metals in CMOS?



Poly cap.



MIM cap.
Metal-Insulator-Metal



MOM cap.
Metal-Oxide-Metal

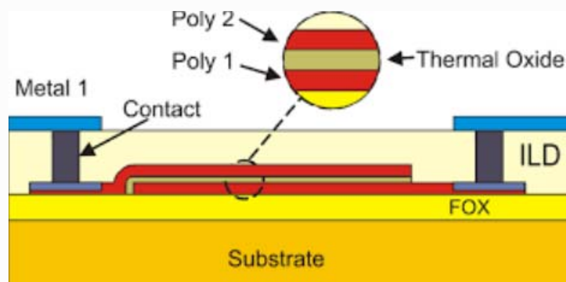
X-Fab Process:

	poly cap	MIM cap	MOM cap
Cap density (fF/μm^2)	0.85	1.25	0.31
Thickness (nm)	41	52	260

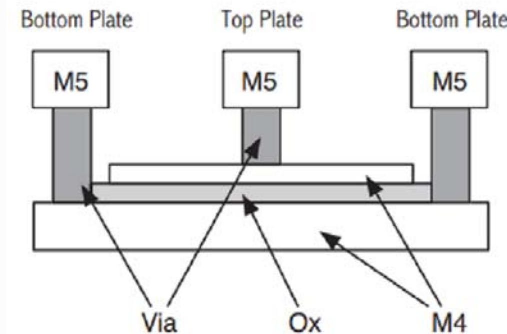
Typical value: 10 fF (10^{-14}) ~ 100 pF (10^{-10})

Different categories of Cap.

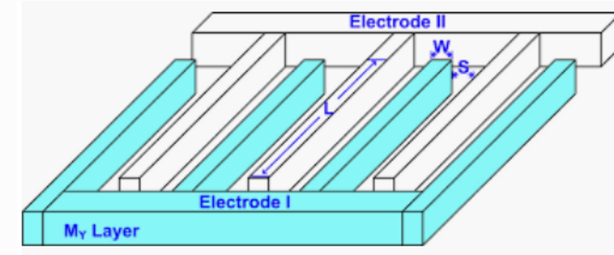
- How to form a parallel plate metals in CMOS?



Poly cap.



MIM cap.
Metal-Insulator-Metal



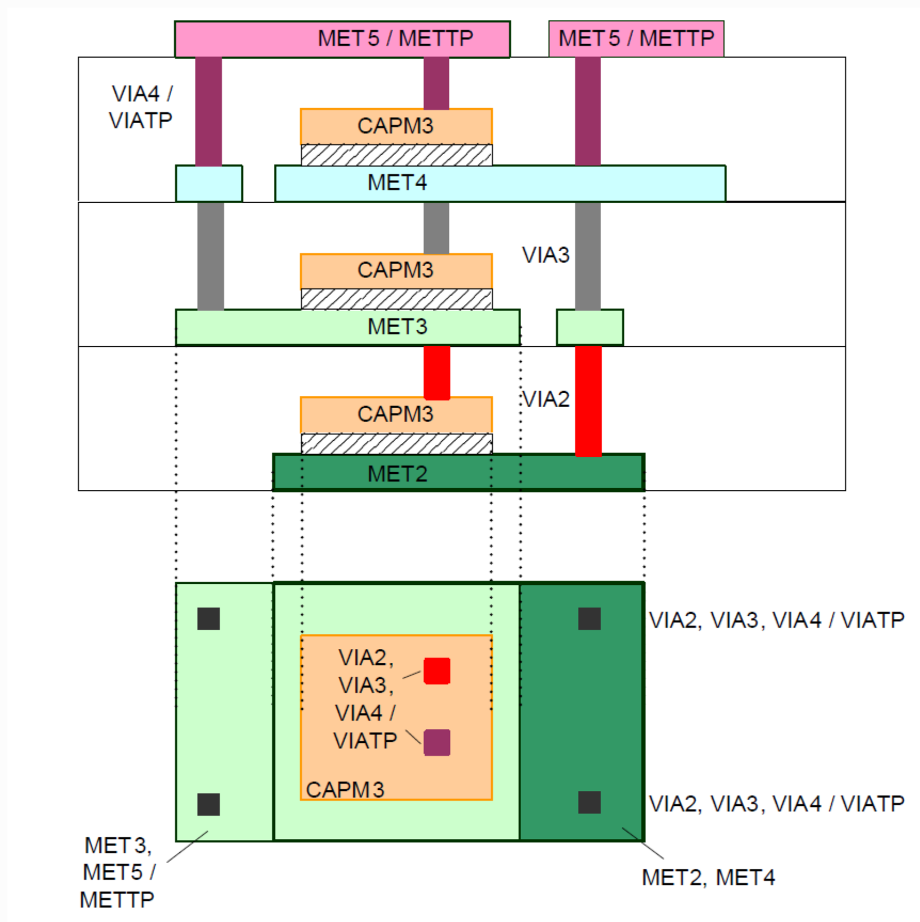
MOM cap.
Metal-Oxide-Metal

Trade-off	poly cap	MIM cap	MOM cap
Extra layer? (Cost)	Yes	Yes	No
Density (Area)	High	High	Low

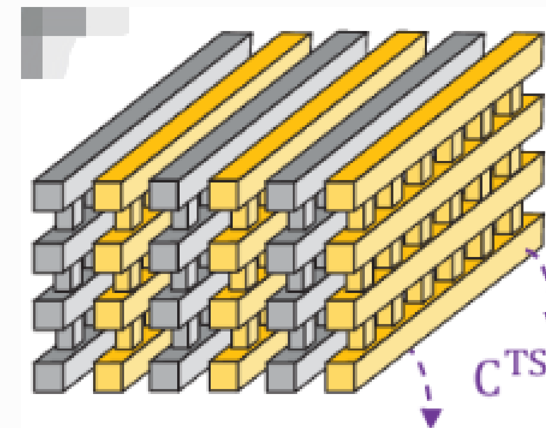
Typical value: 10 fF (10^{-14}) ~ 100 pF (10^{-10})

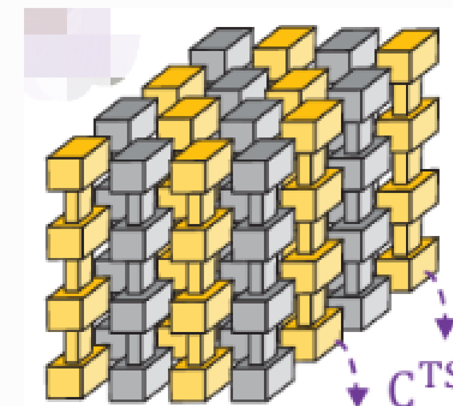
Multi-layer capacitors in CMOS

- Multi-layer tech in MIM and MOM caps.



Multi-layer MIM



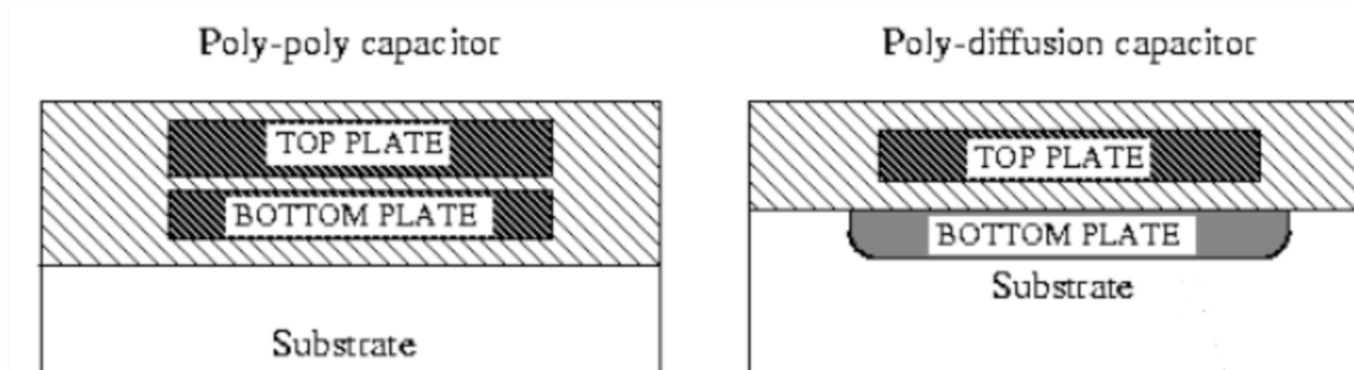


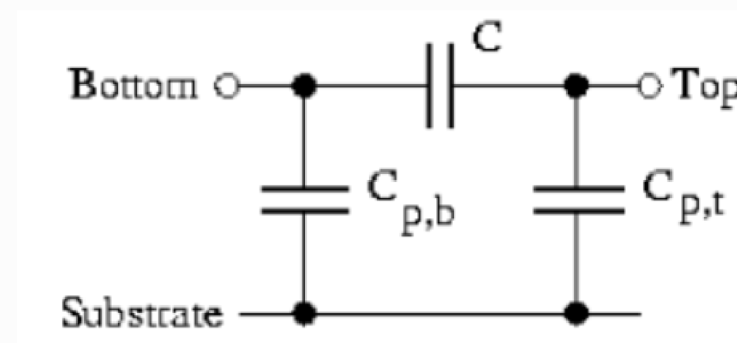
Multi-layer MOM

Intrinsic errors in CMOS cap.

- Plate-substrate parasitic effect (寄生效应)
- Fringed effect (边缘效应)

	diffusion	poly-poly or poly-metal
$C_{p,b}$	0.05C	0.02 C
$C_{p,t}$	0.01C	0.005 C



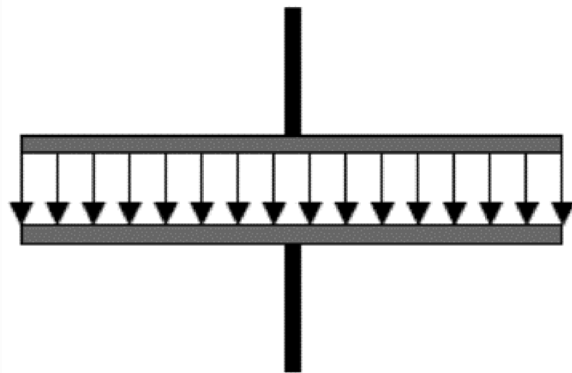


Model including parasitic cap.

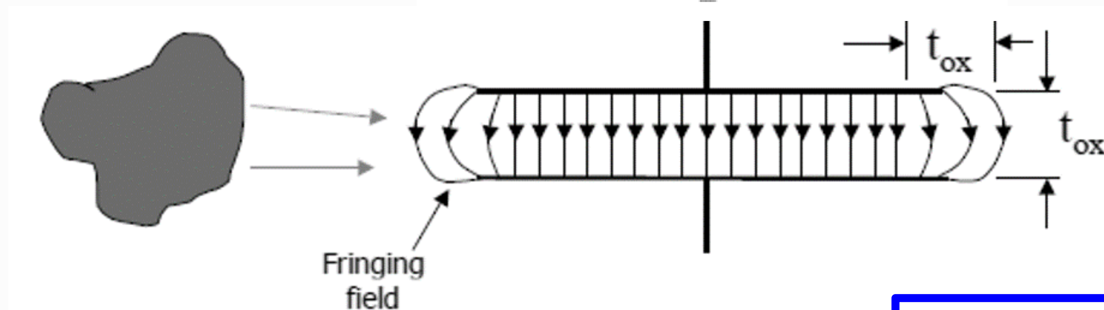
Intrinsic errors in CMOS cap.

- Plate-substrate parasitic effect (寄生效应)
- Fringed effect (边缘效应)

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$



Ideal case



Practical case

10~20% variation!

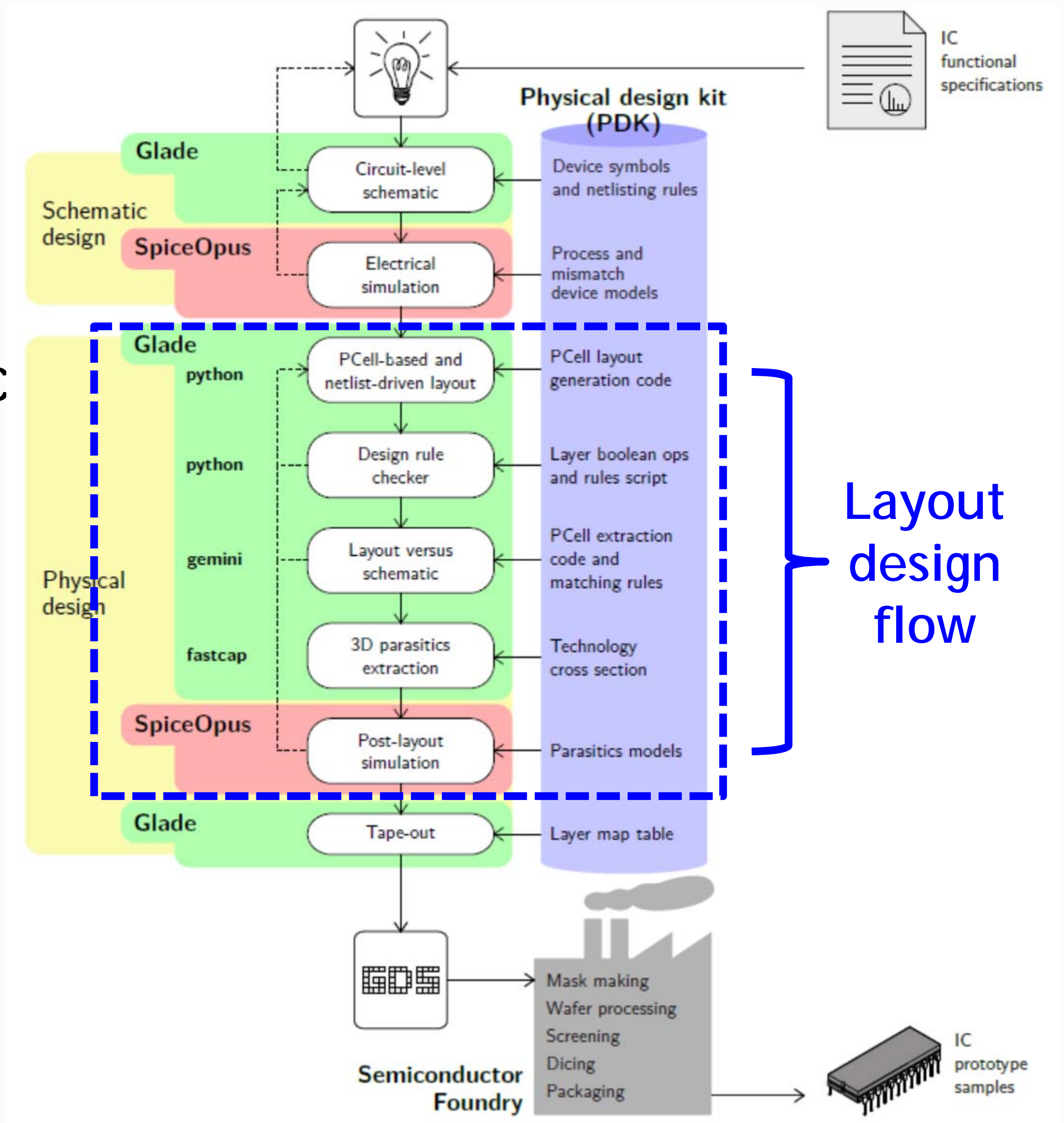
$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} (W - t_{ox})(L - t_{ox}) + C_{fringe}$$

Outline of lecture 1 & 2

- Introduction of Analog Layout
- CMOS process brief
- Design rules
- Basic cells layout
- Design flow of Analog layout (DRC, LVS, PEX)

Layout design flow

- DRC
  - Design rule check
- LVS
  - Layout vs. Schematic
- PEX
  - Parasitic extraction



Summary

- Introduction of layout
  - What is layout? Why we need layout?
- CMOS process brief
- Introduction of design rules
  - Intra layer rules; Inter layer rules
- Layout of basic cells
  - Active (Transistor), Passive (Resistor, Capacitor)
- Layout design flow
  - Layout, DRC, LVS, PEX