



上海交通大学
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lab1 Auto-routing

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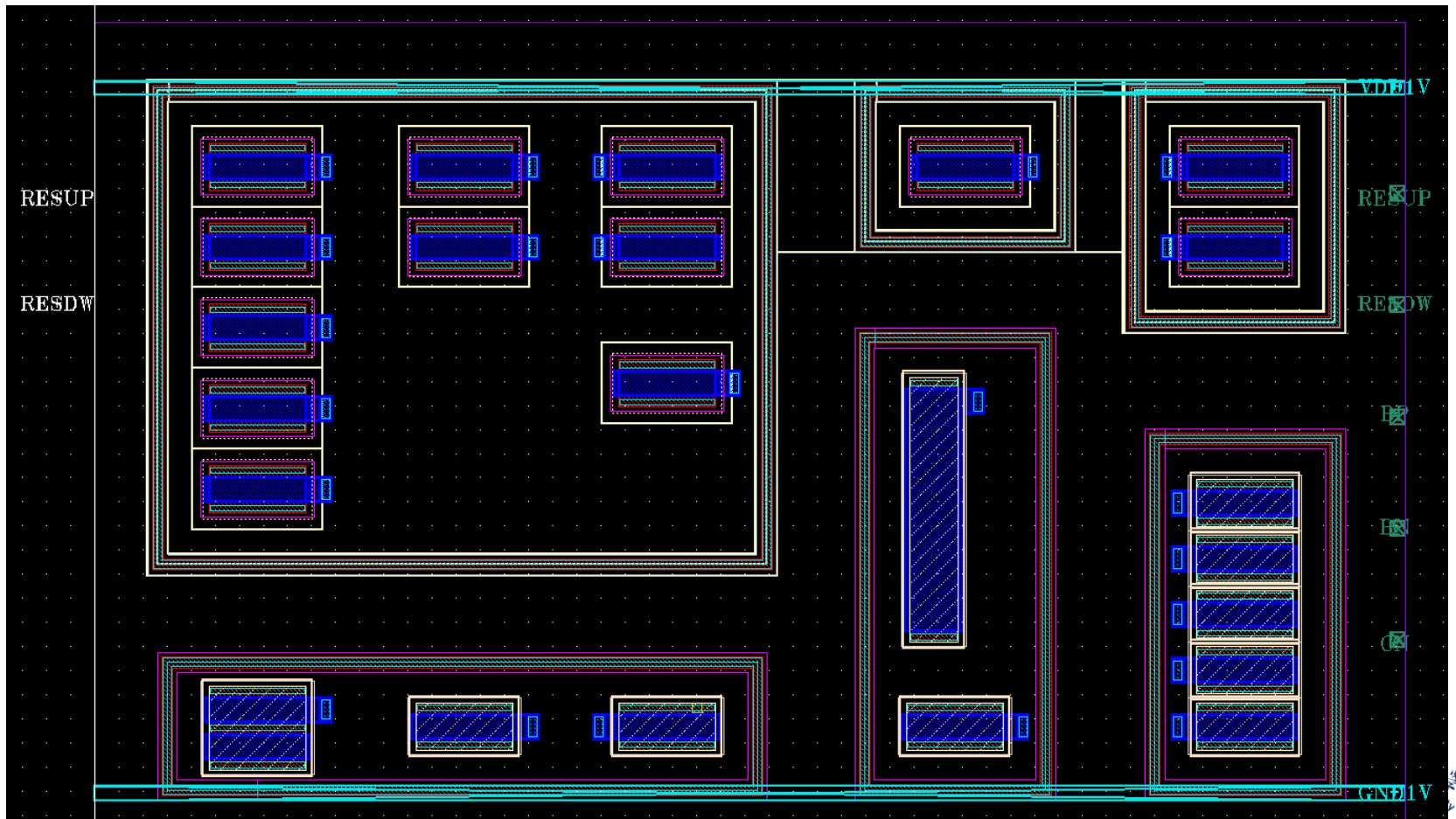
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Outline

- Device & Pin Arrangement
- Auto-routing
- Export & Verification

Device & Pin Arrangement

- 环境：IC5, PDK: TSMC018
- Layout XL



Device & Pin Arrangement

- Place → Pin Placement

Pin Placement: Teaching Current_Bias_Core layout_backup (on cad5. _ □ ×)

Close Defaults Help

Display Control

Display: All All Select edge from layout Link to Layout

Sort: By name

Select: []

Pin Name	Edge	Order	Pitch	Status	Type	Layer
BN	right	4			IO	METAL3
BP	right	3			IO	METAL3
CN	right	5			IO	METAL3
GND1V	H-Rail	6		M	IO	METAL1
RESDW	right	2			IO	METAL3
RESUP	right	1			IO	METAL3
VDD1V	H-Rail	0		M	IO	METAL1

Iterated Pins

Interleave

Expand

Collapse

All Selected

Change Order

Move pins

Swap order

Place pins as in:

Schematic view

Template file ...

HRail VRail

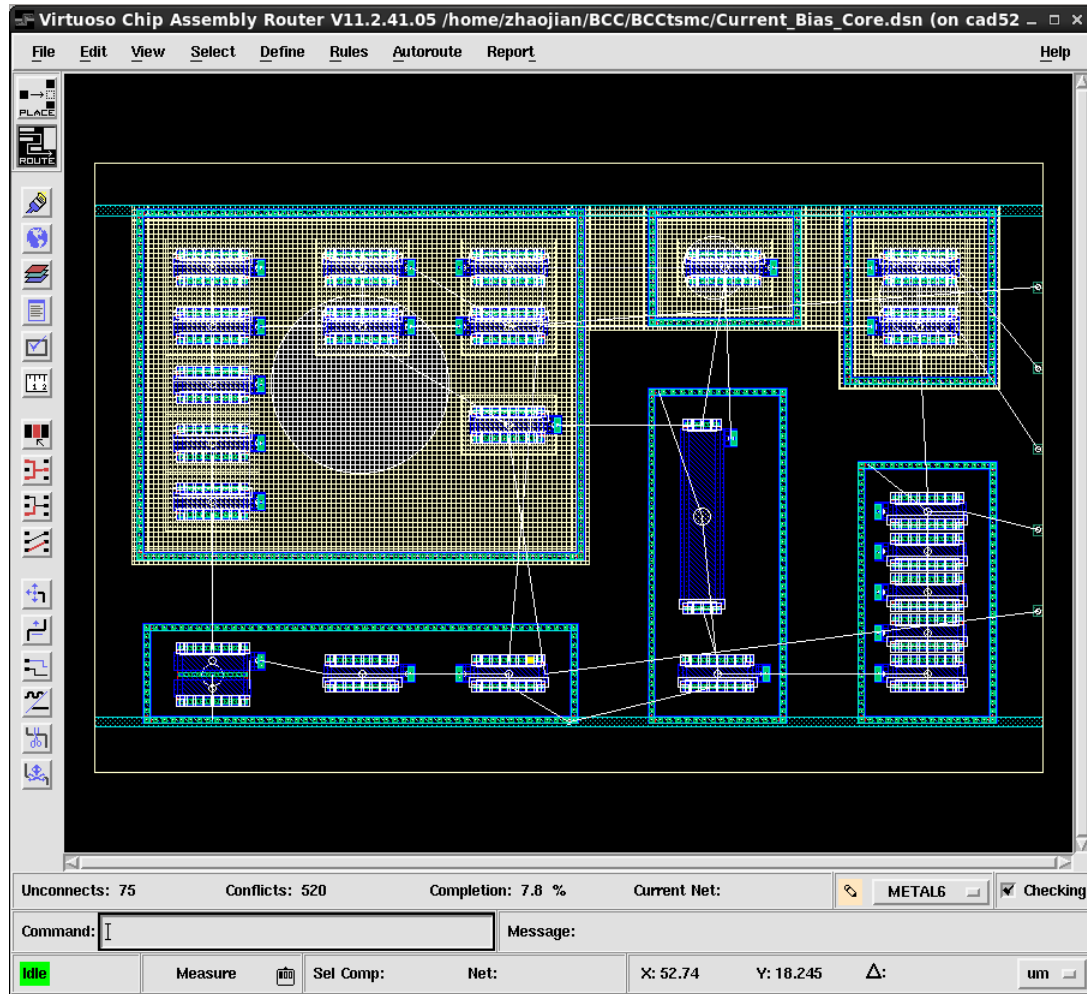
Edge Order Pitch: Location

Any [] [] Fix at Placed Location

Select edge from layout Apply

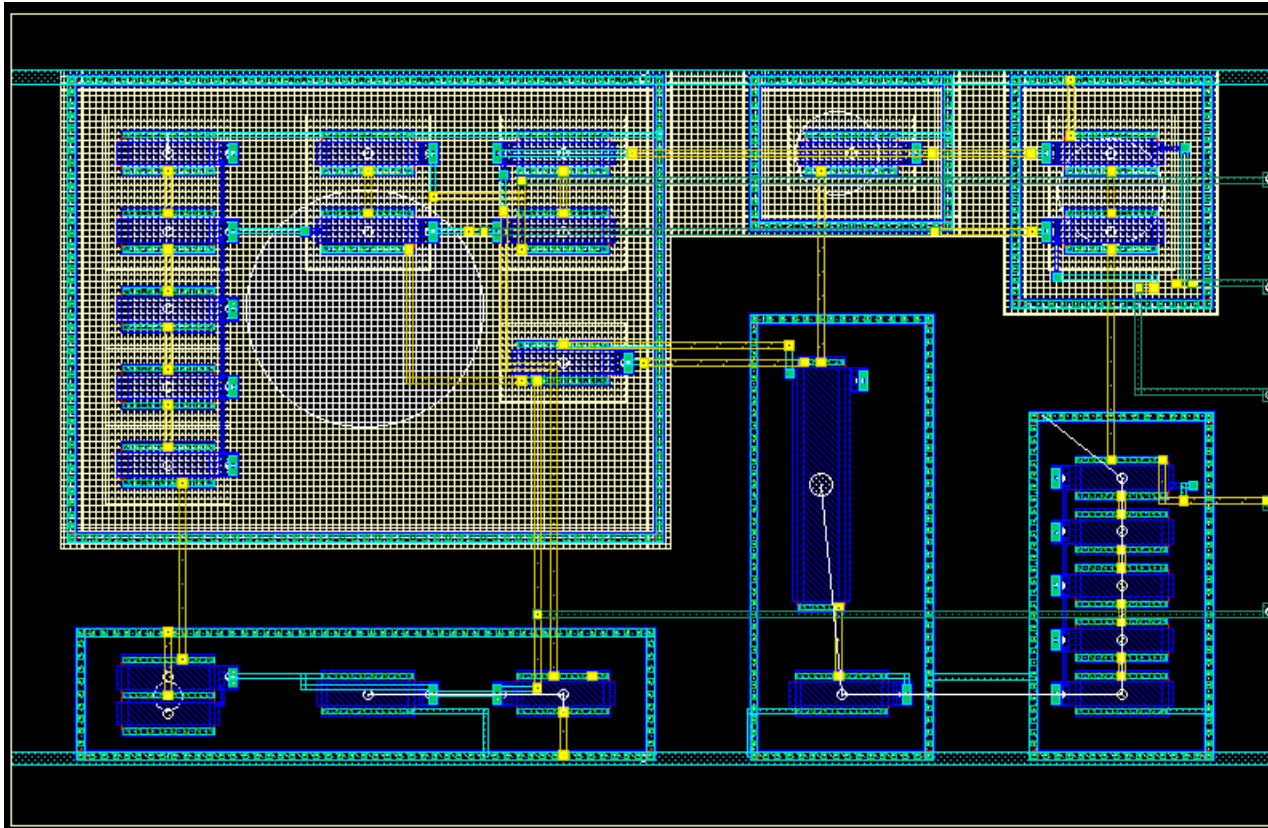
Auto-routing

- Routing → Export to router
- Select PDK rules



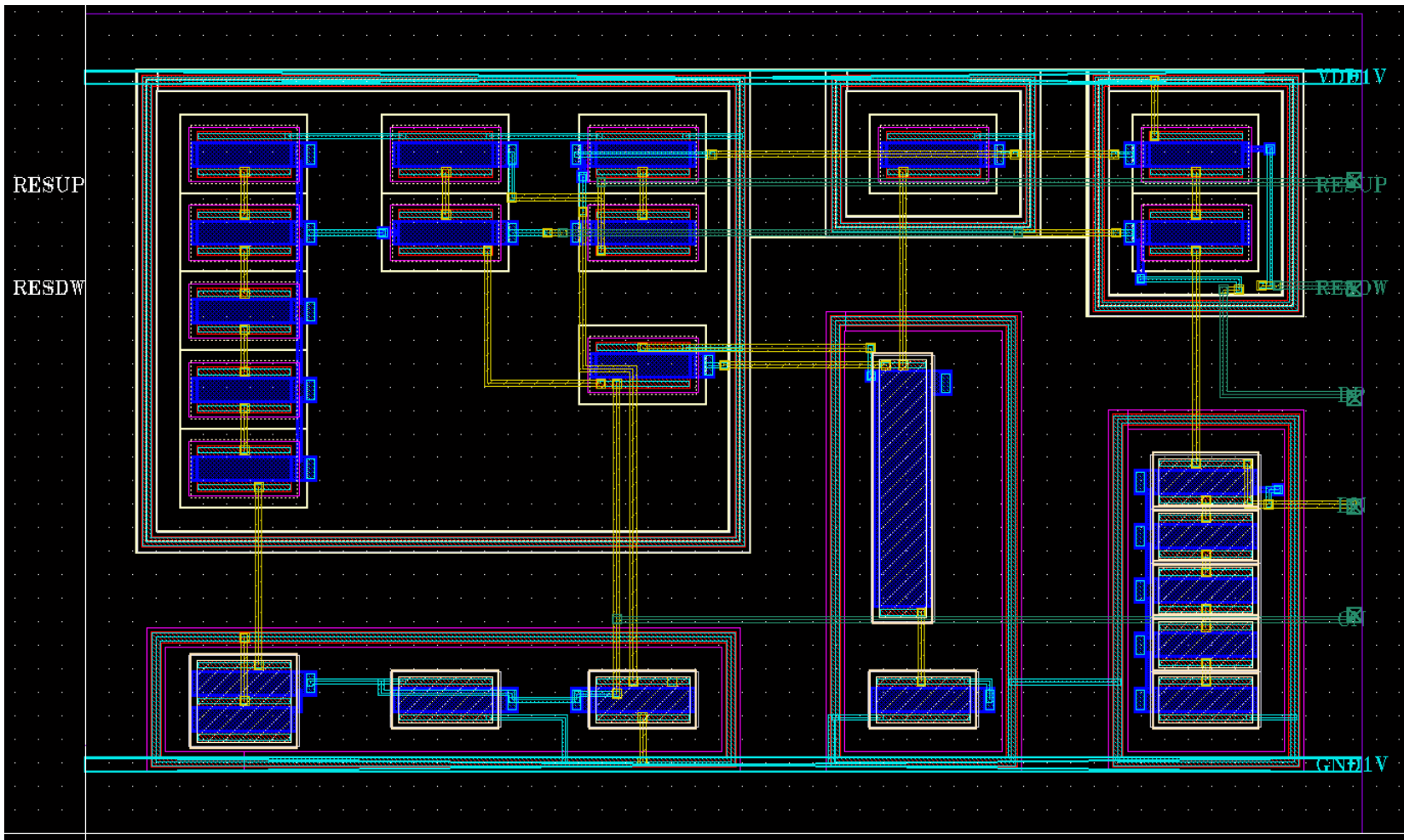
Auto-routing

- Routing → Export to router
- Select PDK rules
- → Detailed Route



Export & Verification

- File → Write → Session, manually correct the errors
- Run LVS, DRC...





Thanks!

