



上海交通大學
SHANGHAI JIAO TONG UNIVERSITY



lab1 Inverter design

Luo Jing

Department of Micro-nano electronics
Shanghai JiaoTong University
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Self-Introduction

- TA: 罗京/luo jing
- 实验室地址/address of lab: 微电子大楼404室
/room 404 of Micro-electronics building
- 邮箱/email: luojing@sjtu.edu.cn
- 电话/phone number: 19822791625

Outline

- Server login
- Schematic design
- Pre-Simulation
- Layout design
- Post-Simulation
- Some shortcut keys

Server login

- For Ubuntu, (开机密码: 123456)
- Step 1: 打开Terminal,

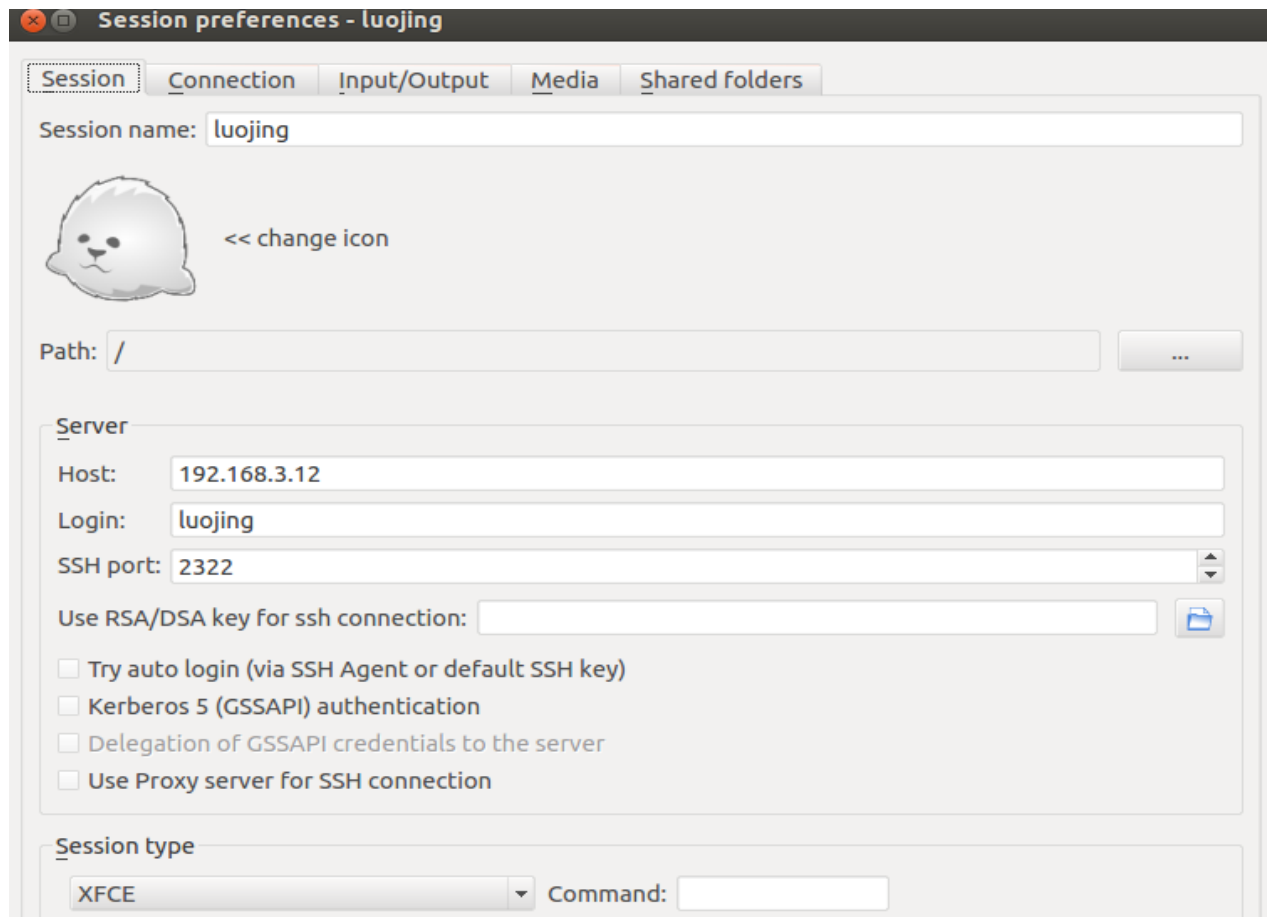
```
microe@microe71:~$ ssh luojing@192.168.3.12 -p 2322
```

初始密码: 每个人的姓名拼音;

根据提示修改password;

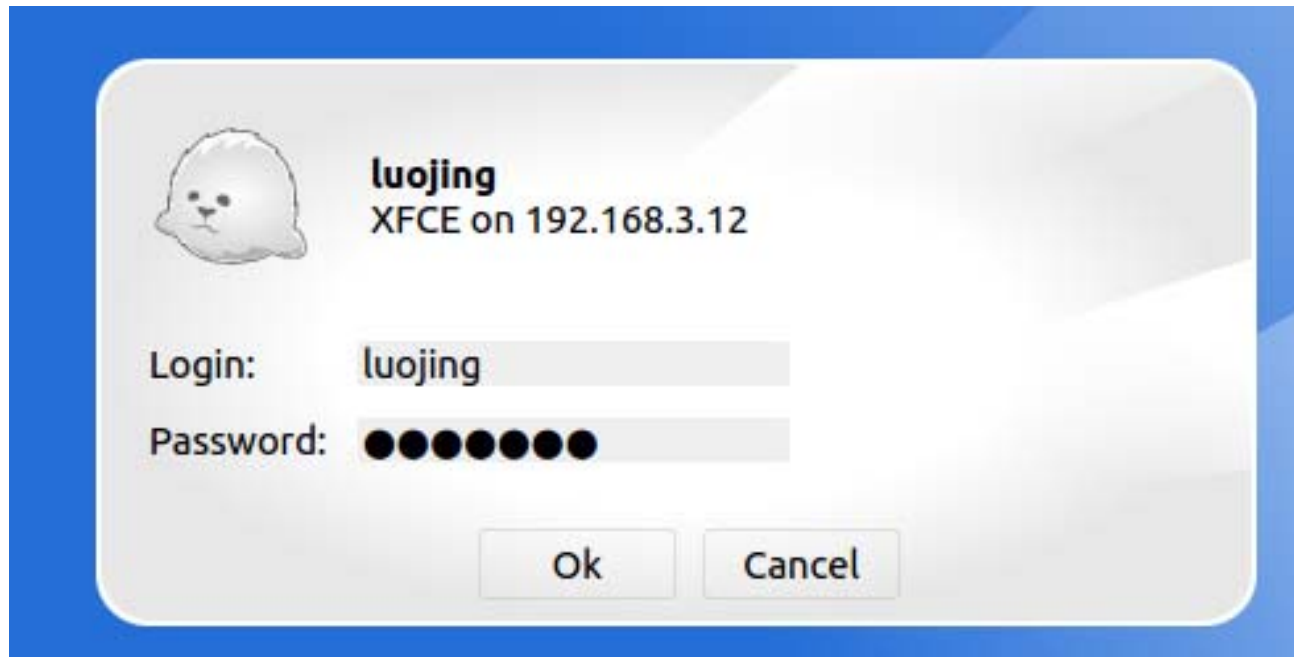
Server login

- Step 2: 打开新的Terminal, 输入 x2goclient, 进入x2goclient之后, 打开新的session, 设置如下:



Server login

设置好之后，点击该session，输入密码即可登录；



Server login

- Step 3: 登录进server之后，打开Terminal(注意这里不是Ubuntu的terminal)，输入下面的命令：

```
$ bash
```

```
luojing@microe:~/Desktop$ cd ..
```

```
luojing@microe:~$ cd project_xh035_1022/  
luojing@microe:~/project_xh035_1022$ source /eda/bashrc_ic616  
luojing@microe:~/project_xh035_1022$ virtuoso
```

即可打开cadence

Server login

- For Windows,

直接打开putty,

设置好host name: 192.168.3.12, port:2322, 点击ok

然后login as: 姓名拼音

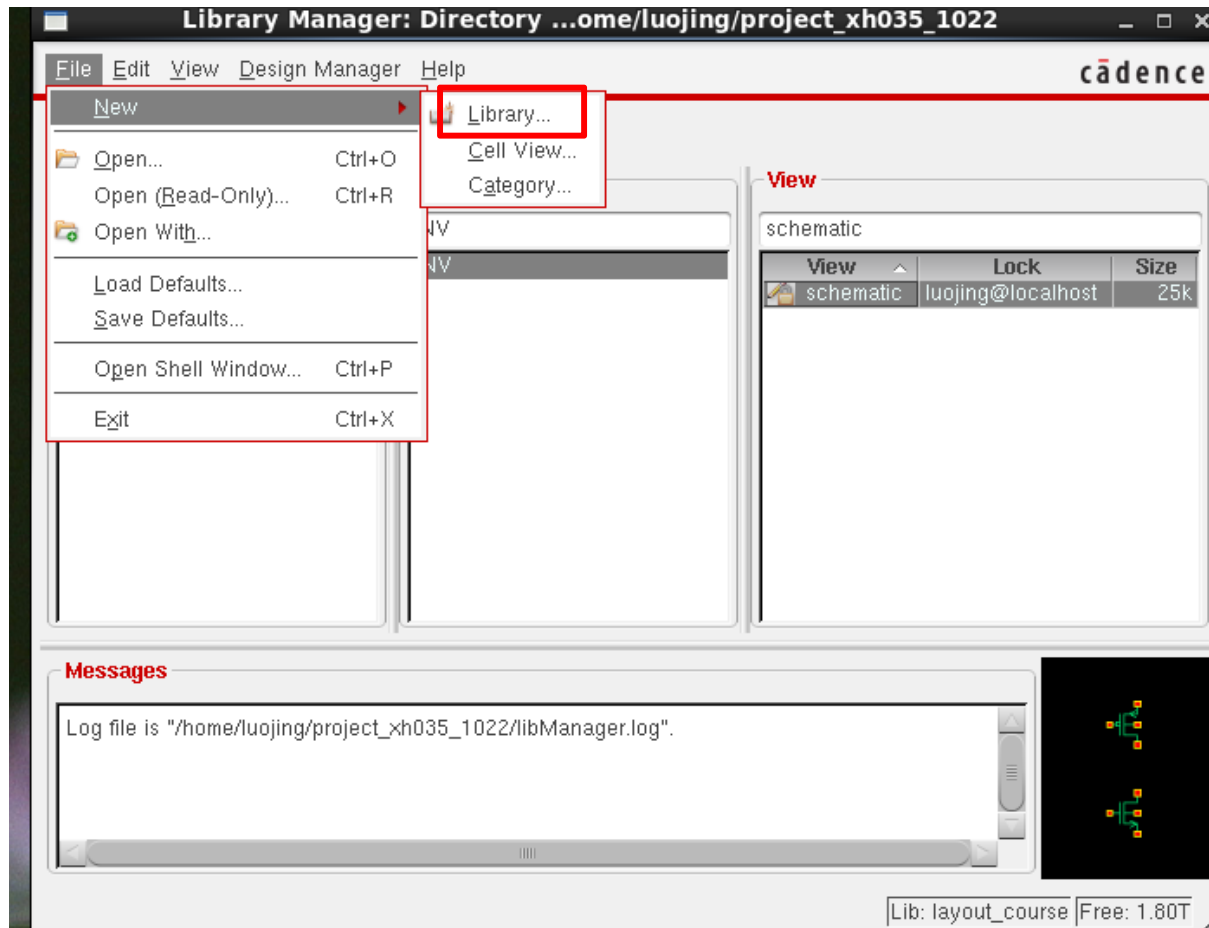
Password: 姓名拼音

按照提示修改密码即可;

- 在桌面上打开X2Go client, 之后的步骤和前面的设置一样

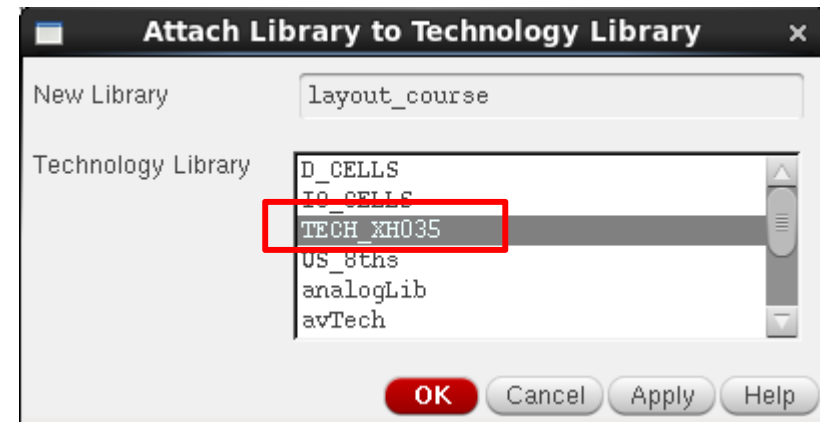
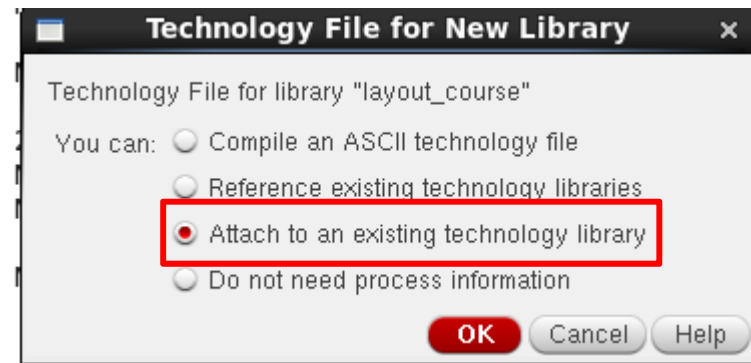
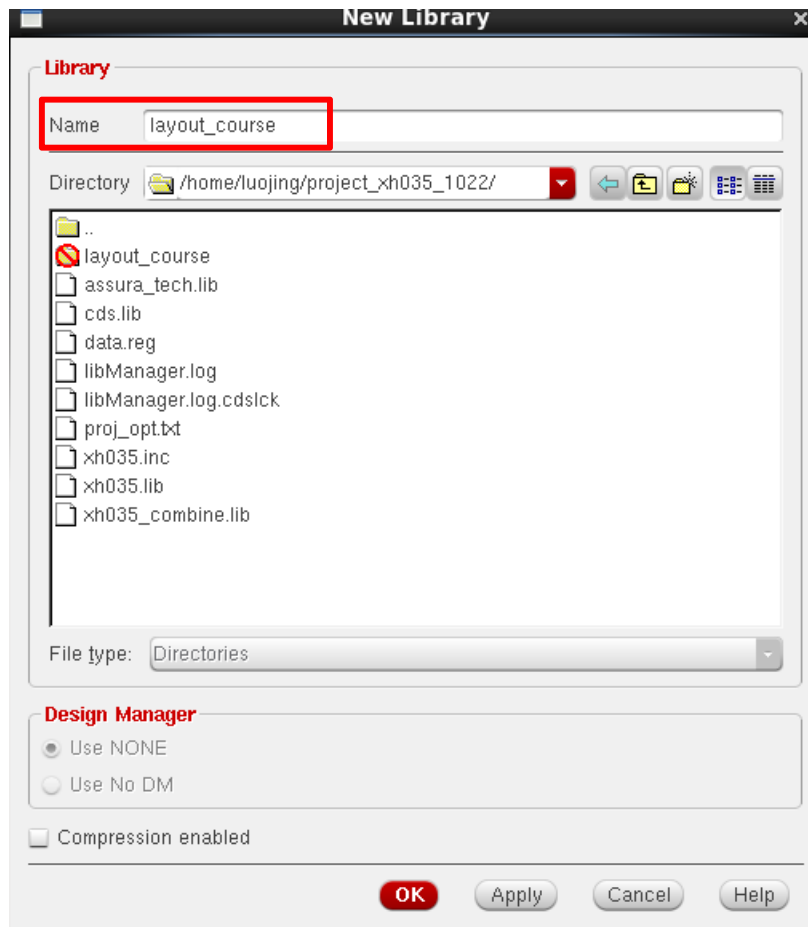
Schematic design

■ Create a library



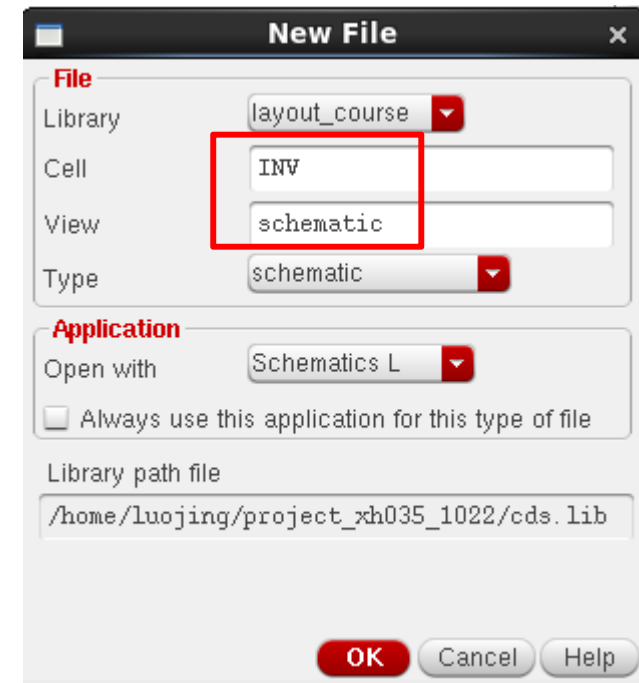
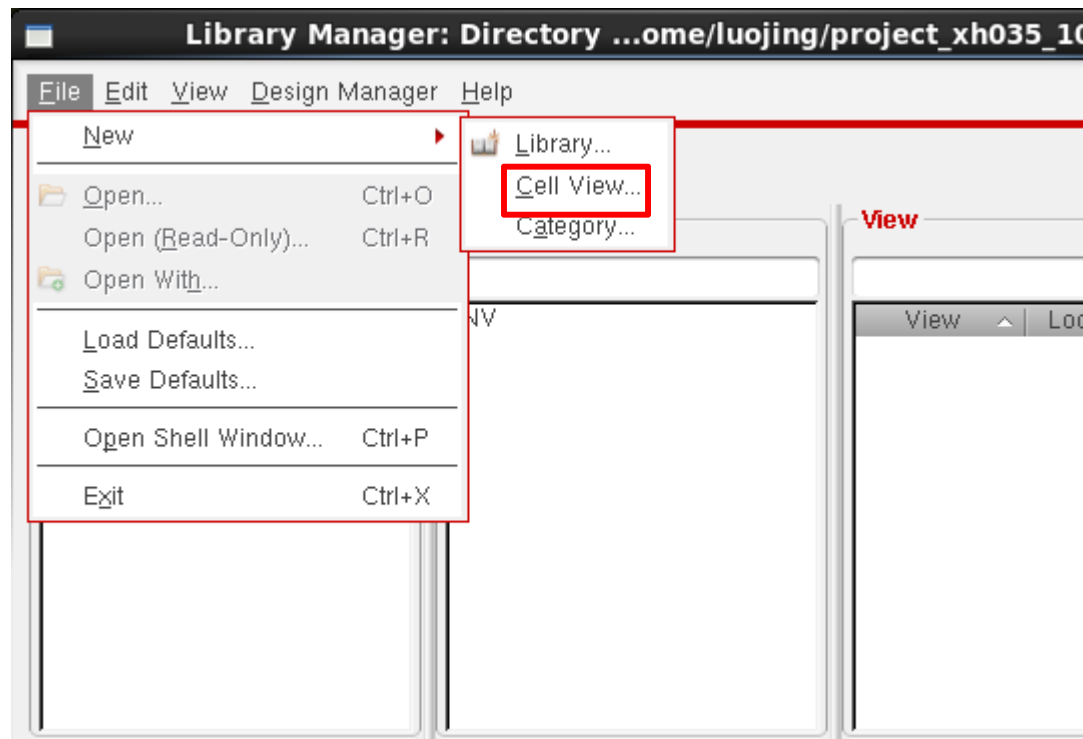
Schematic design(cont'd)

- Name the library, attach to a tech lib(TECH_XH035)



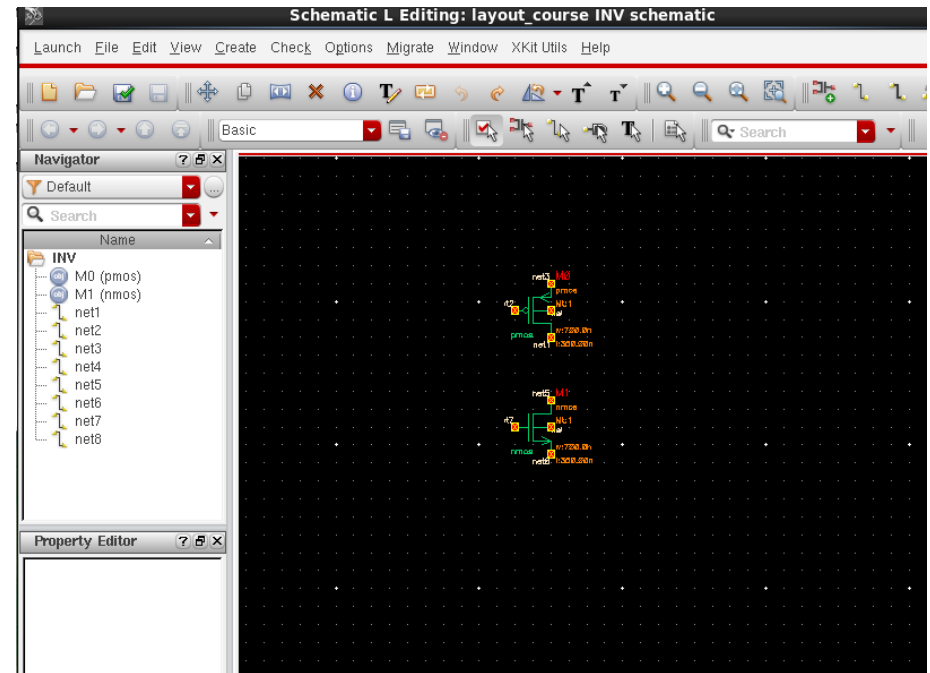
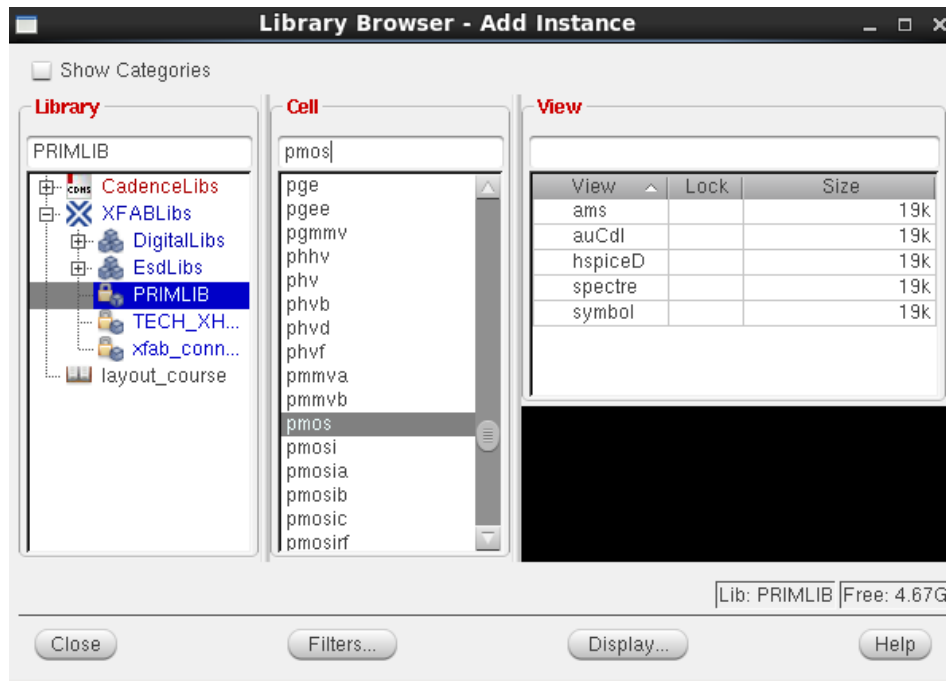
Schematic design(cont'd)

- Create a schematic file in library “layout_course”



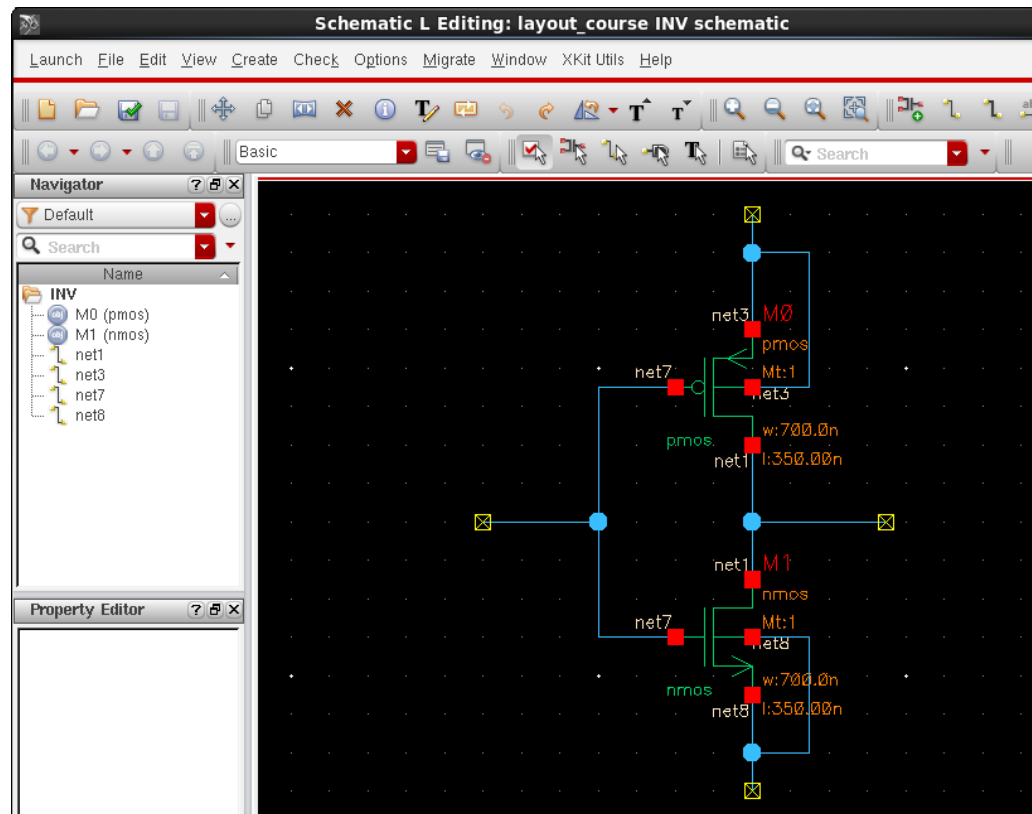
Schematic design(cont'd)

- Add instances(shortcut key — i)



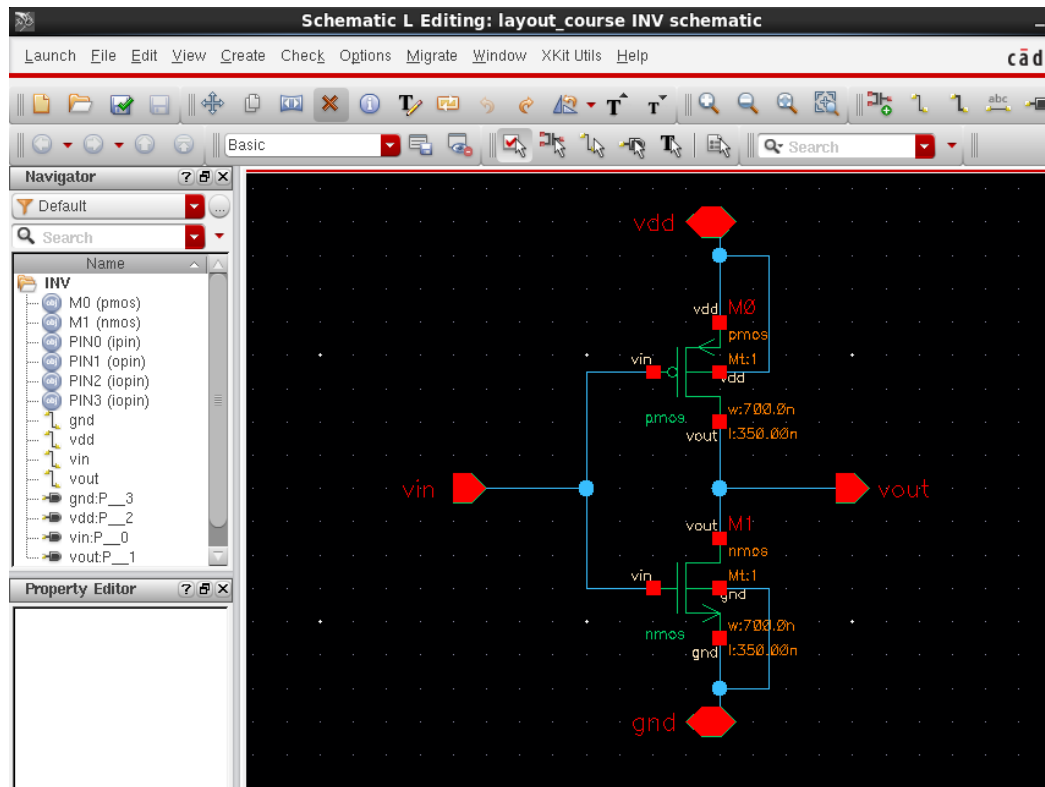
Schematic design(cont'd)

- Add wires(shortcut key — w)



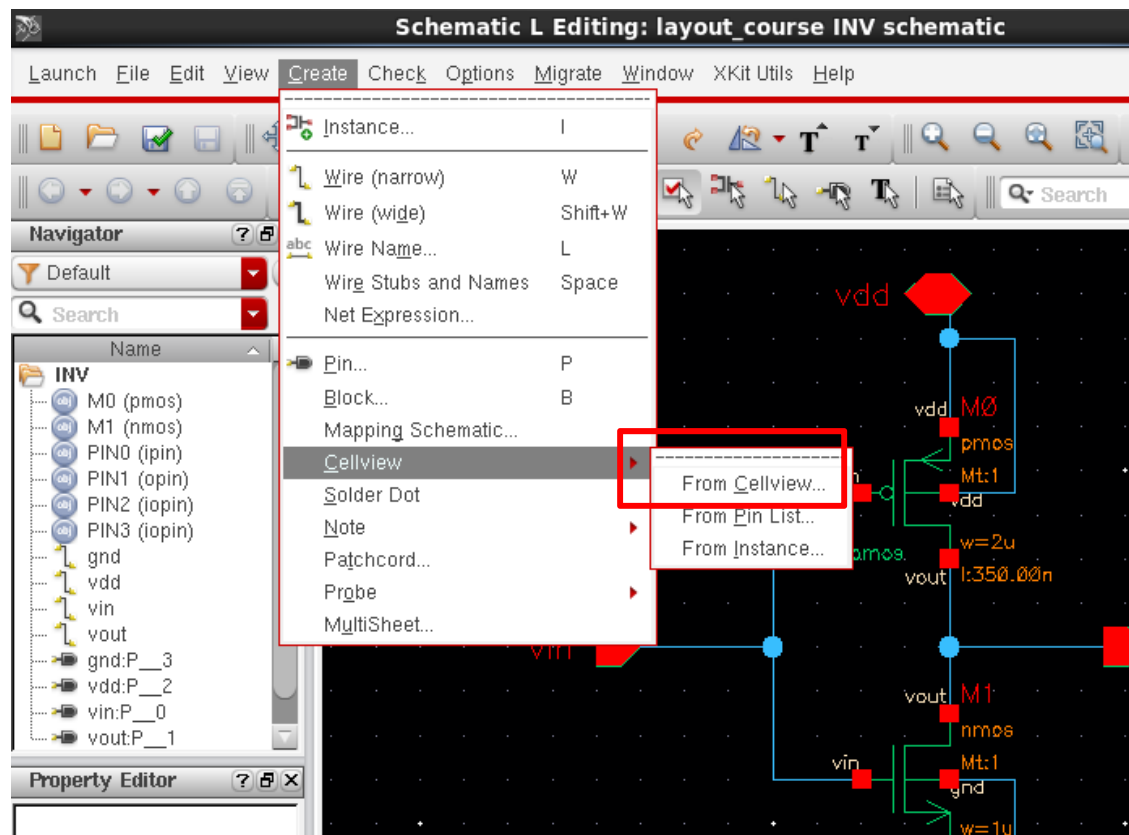
Schematic design(cont'd)

- Add pins(shortcut key — p)



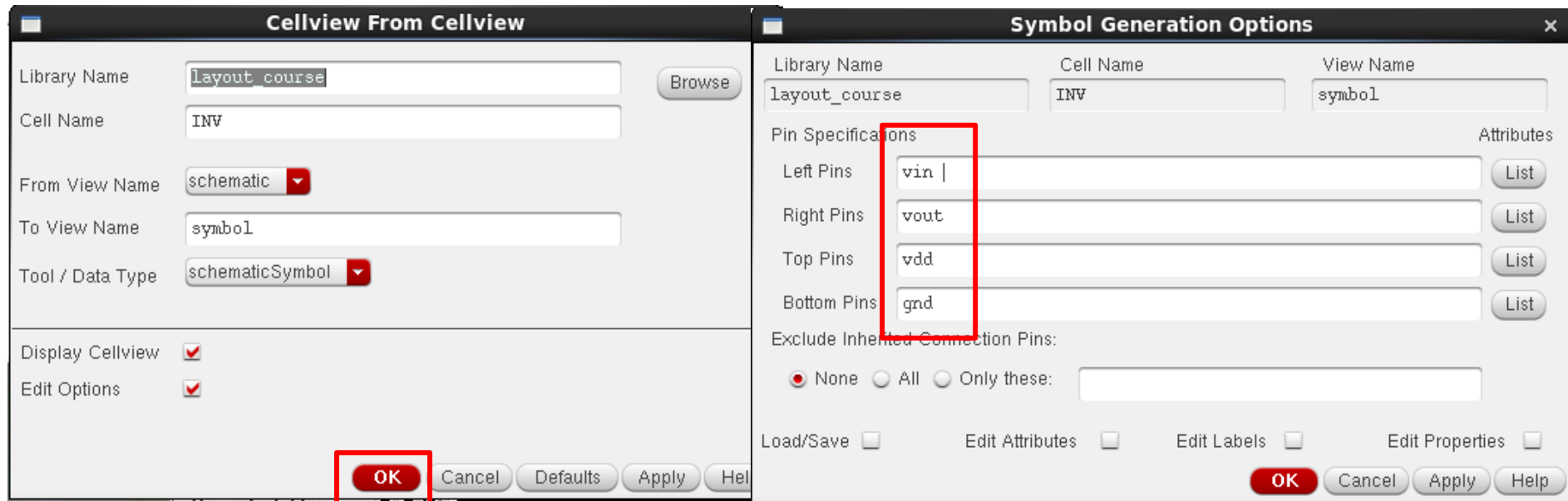
Schematic design(cont'd)

- Create a symbol of the schematic



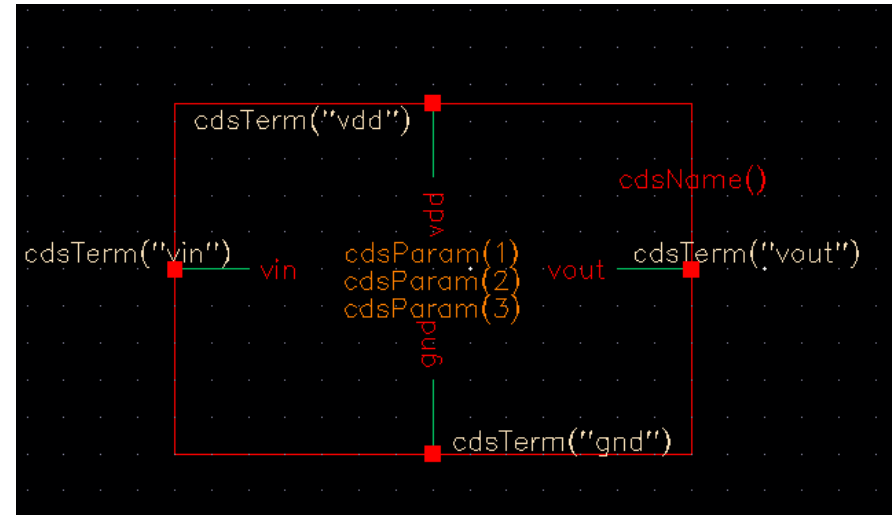
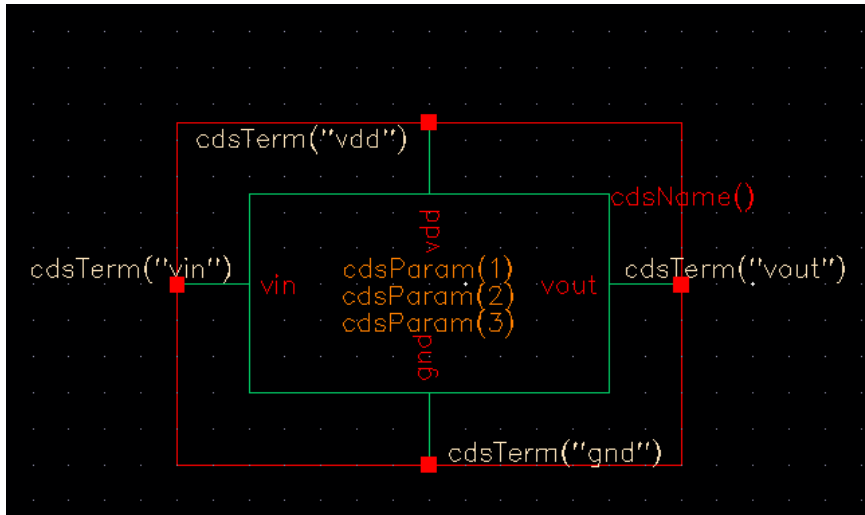
Schematic design(cont'd)

- Place pins in different directions



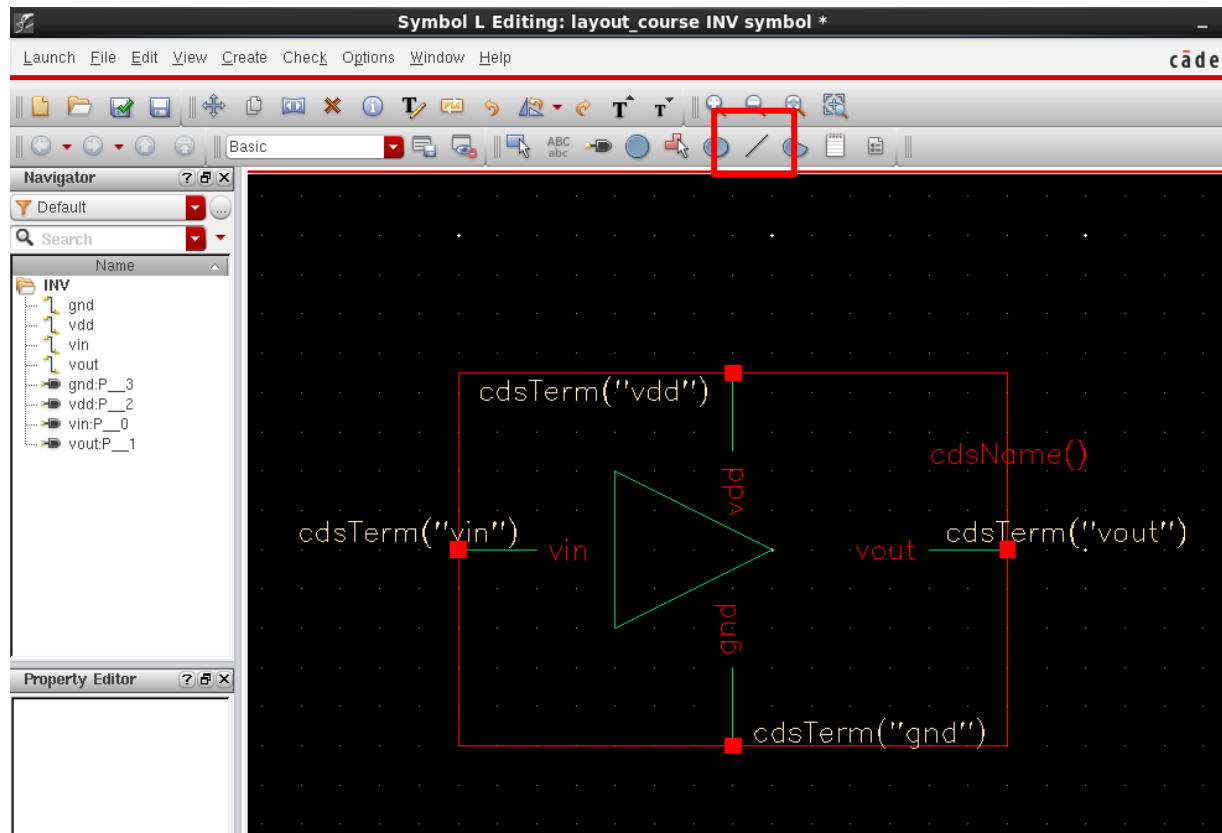
Schematic design(cont'd)

- Change shape of symbol(shortcut key — delete)



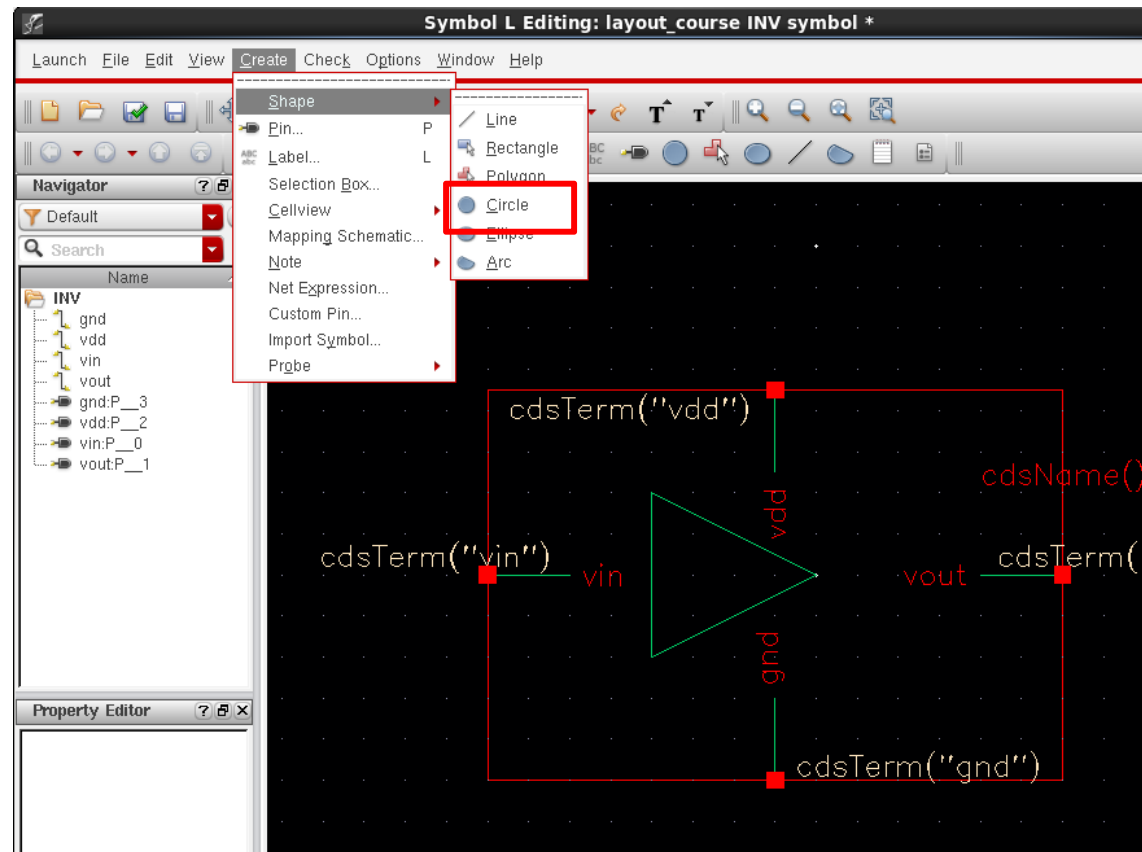
Schematic design(cont'd)

- Draw a shape you like



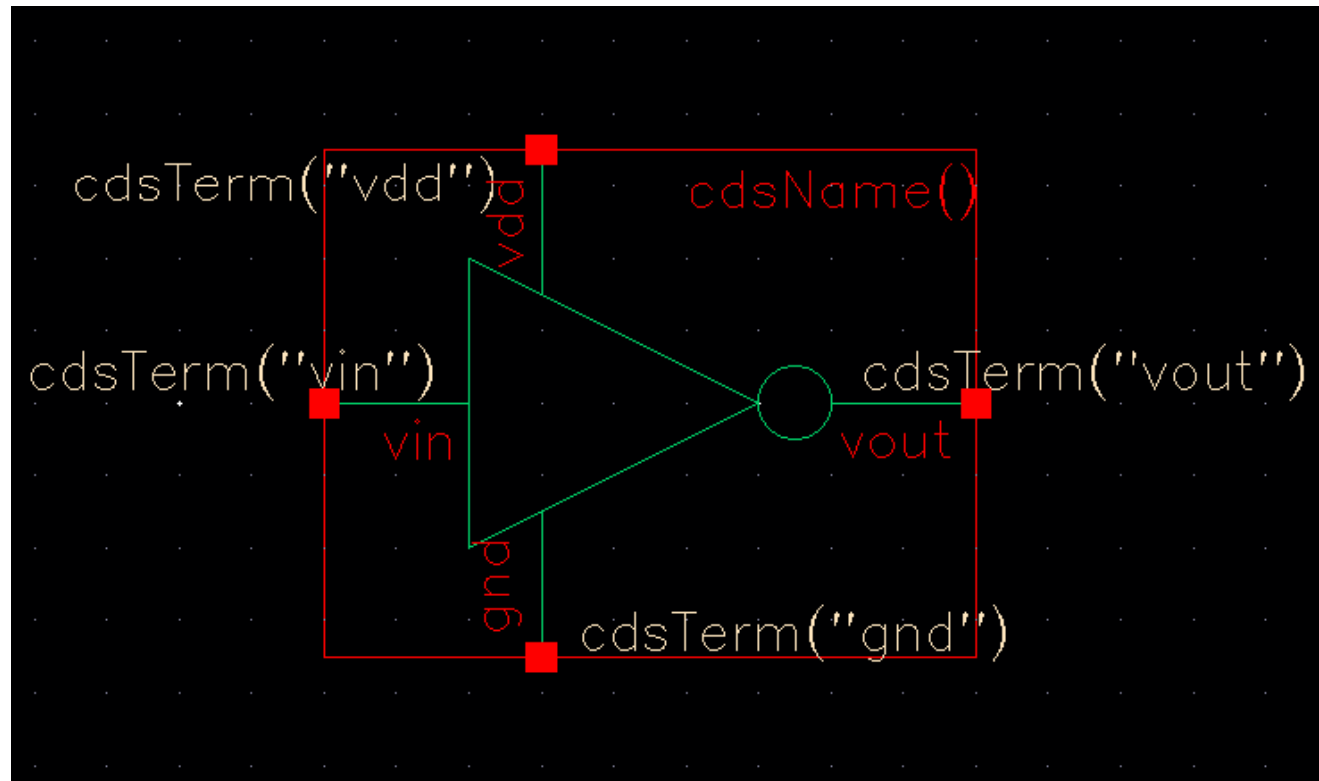
Schematic design(cont'd)

- Draw a circle



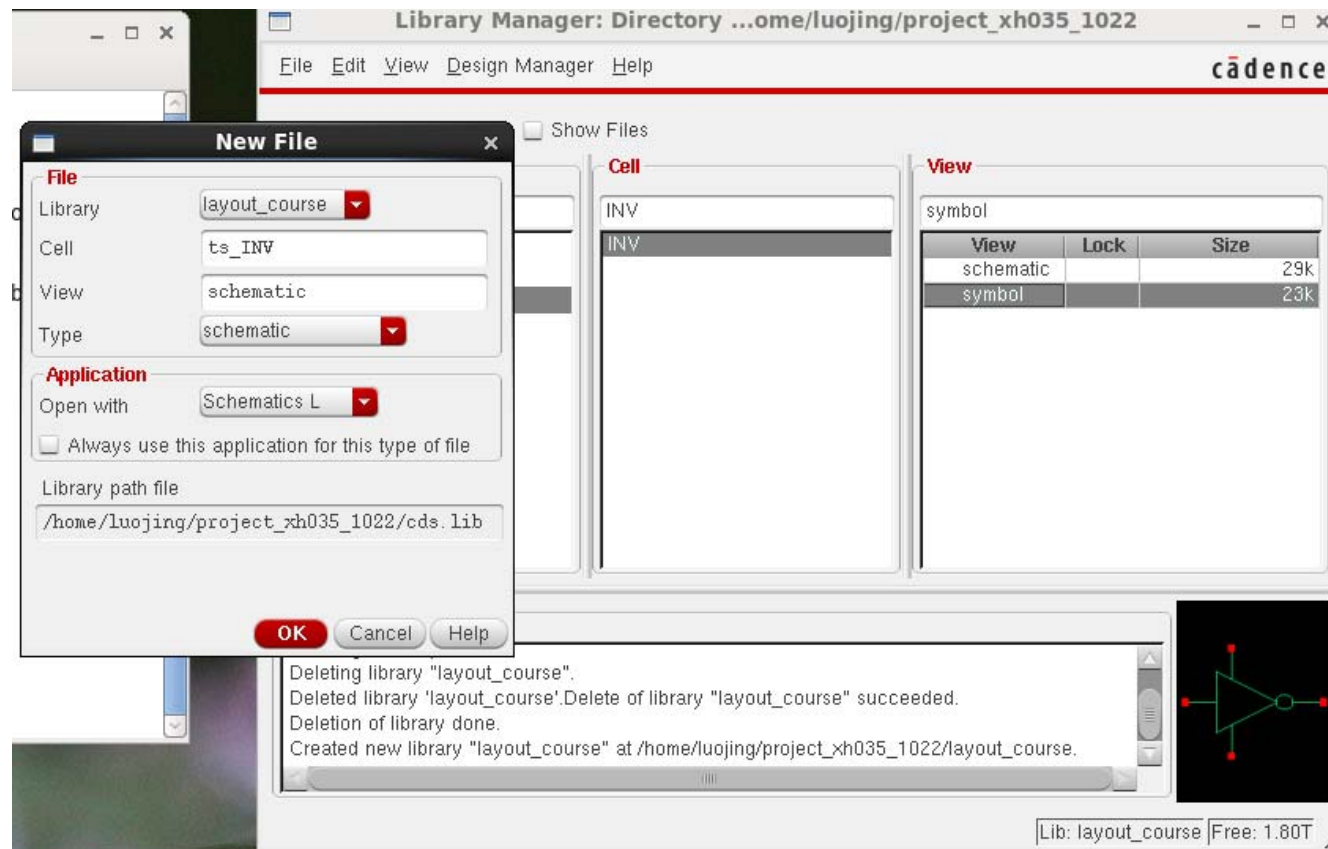
Schematic design(cont'd)

- Get the final shape like this



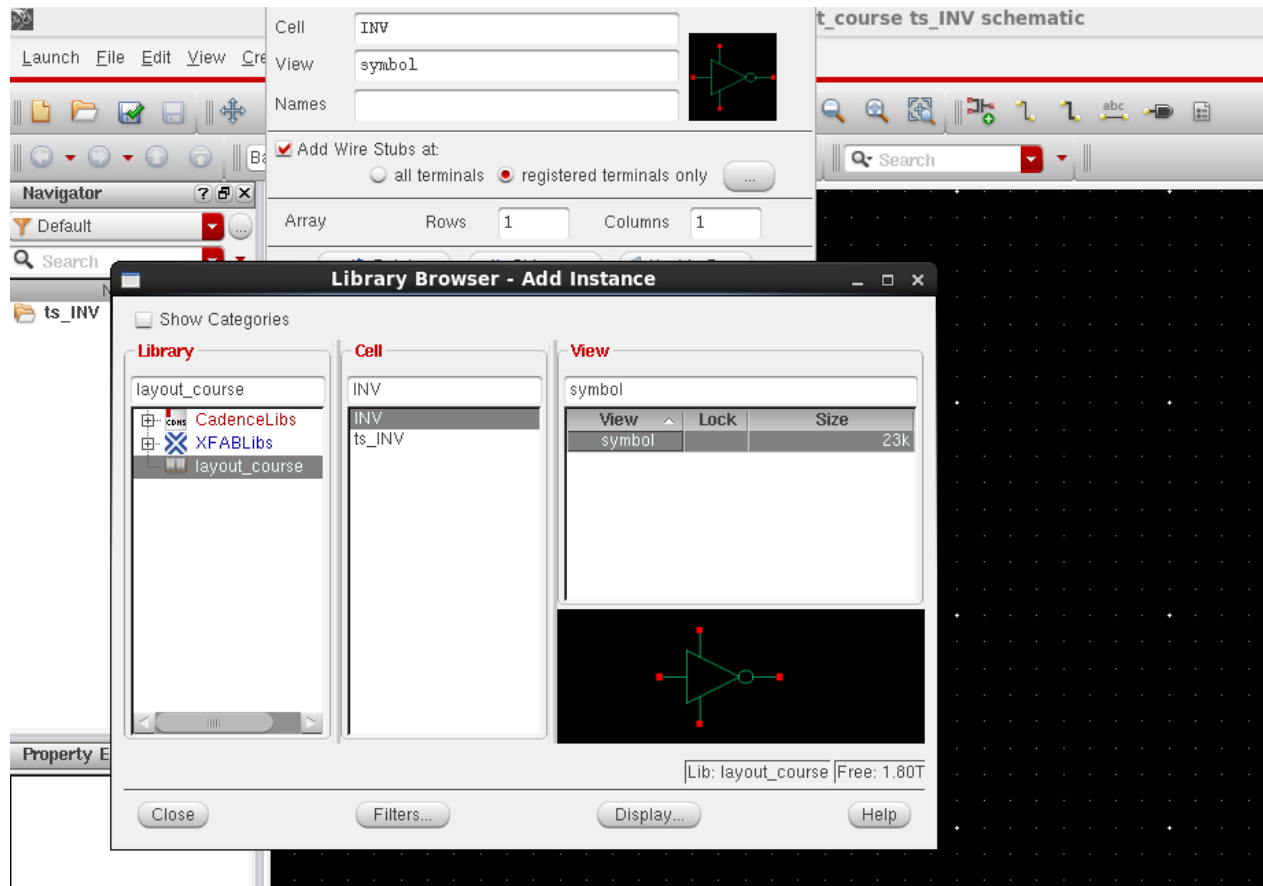
Pre-Simulation

- Create testbench schematic



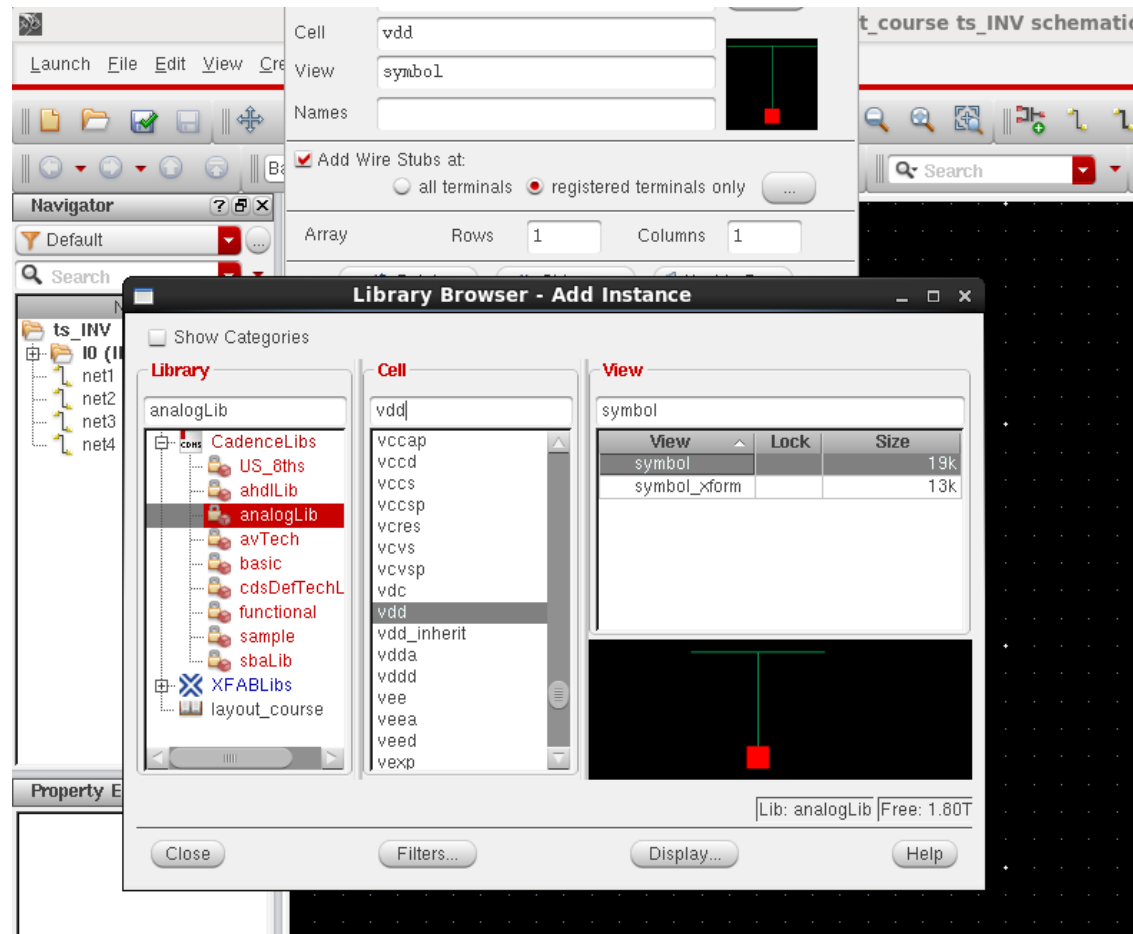
Pre-Simulation(cont'd)

- Add instances(shortcut key — i)



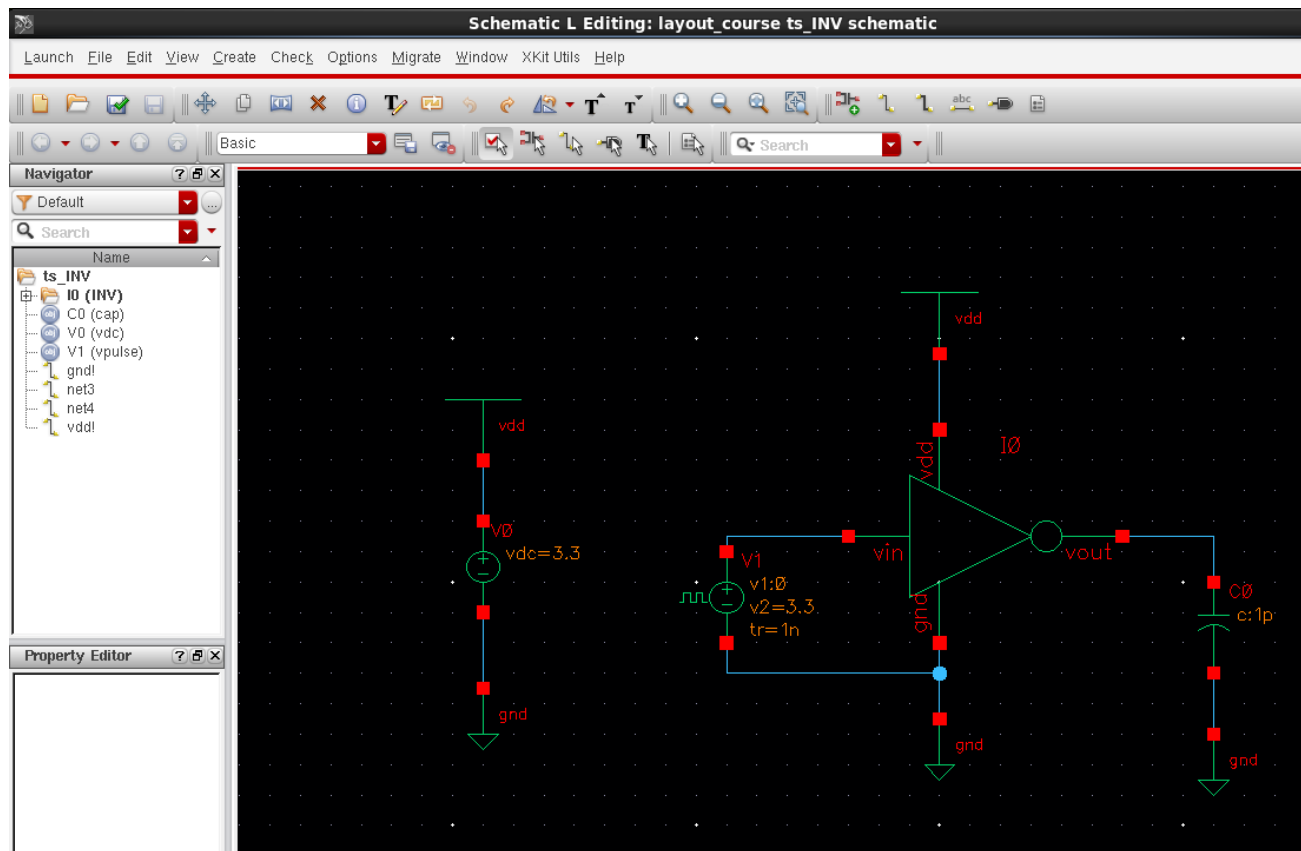
Pre-Simulation(cont'd)

- Add voltage source(shortcut key — i)



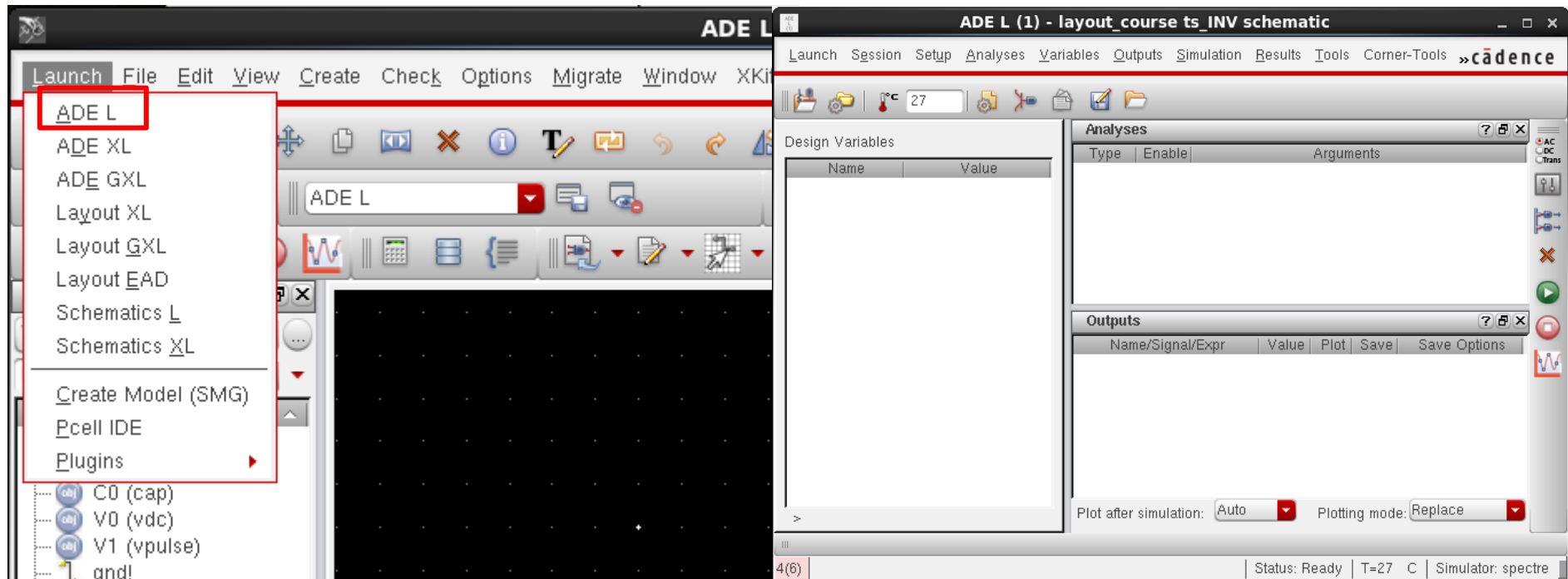
Pre-Simulation(cont'd)

- Connect all the parts and get final schematic



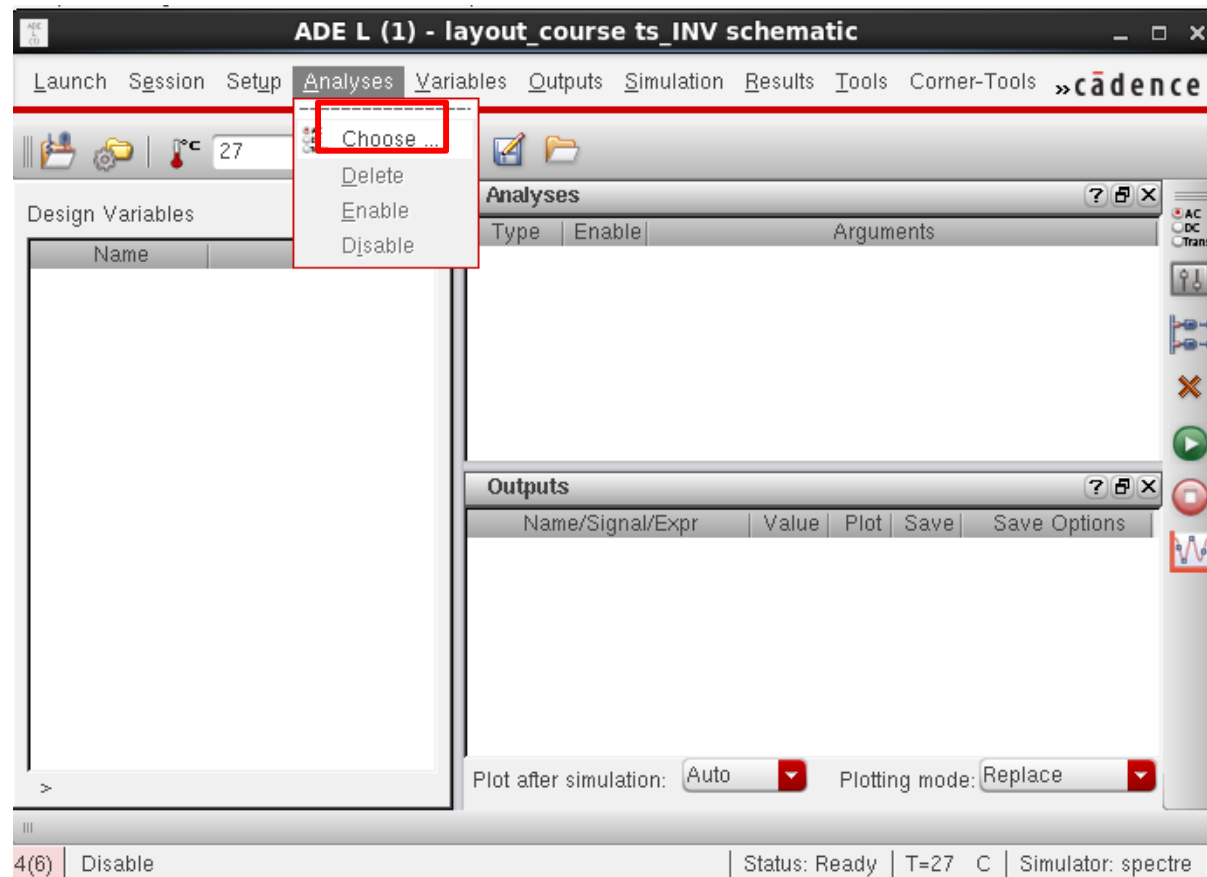
Pre-Simulation(cont'd)

- Start simulation, open ADE



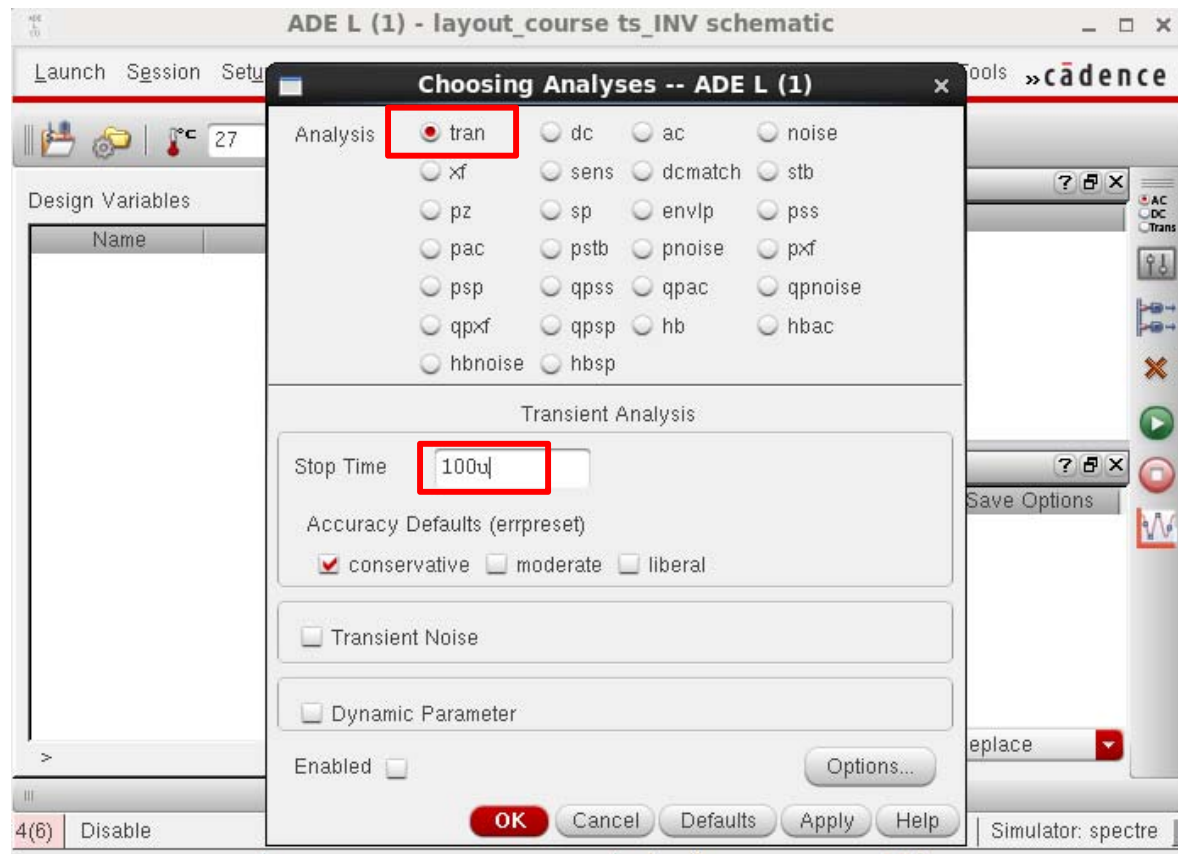
Pre-Simulation(cont'd)

- Choose analysis you want to do



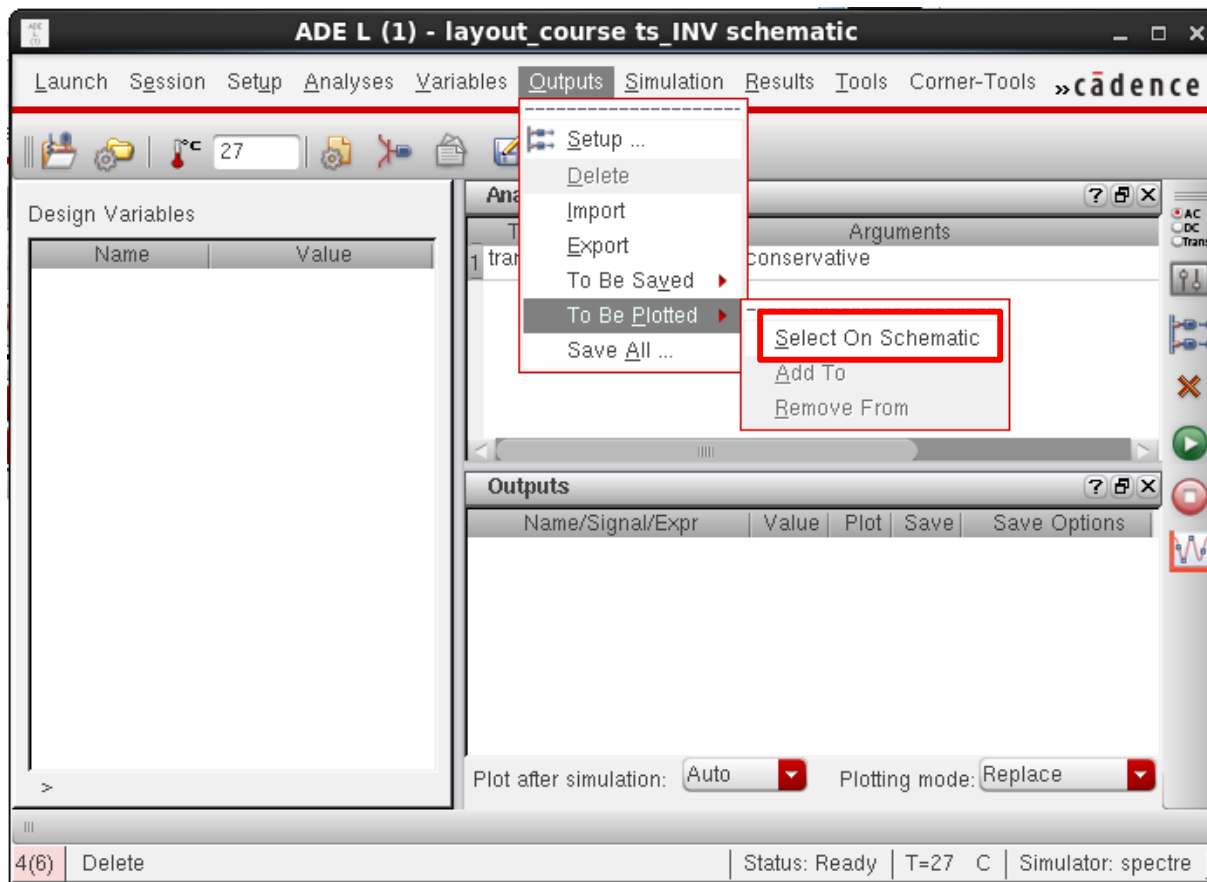
Pre-Simulation(cont'd)

- We choose tran analysis



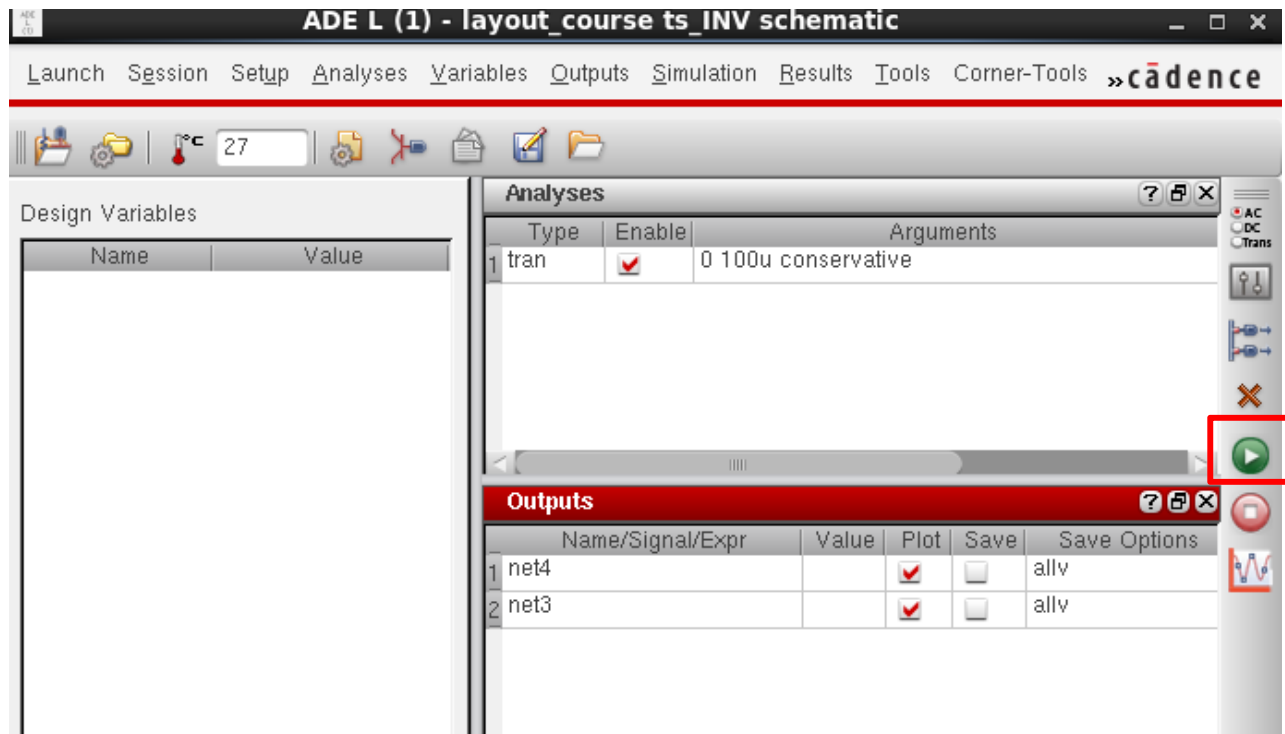
Pre-Simulation(cont'd)

- Select signals to display



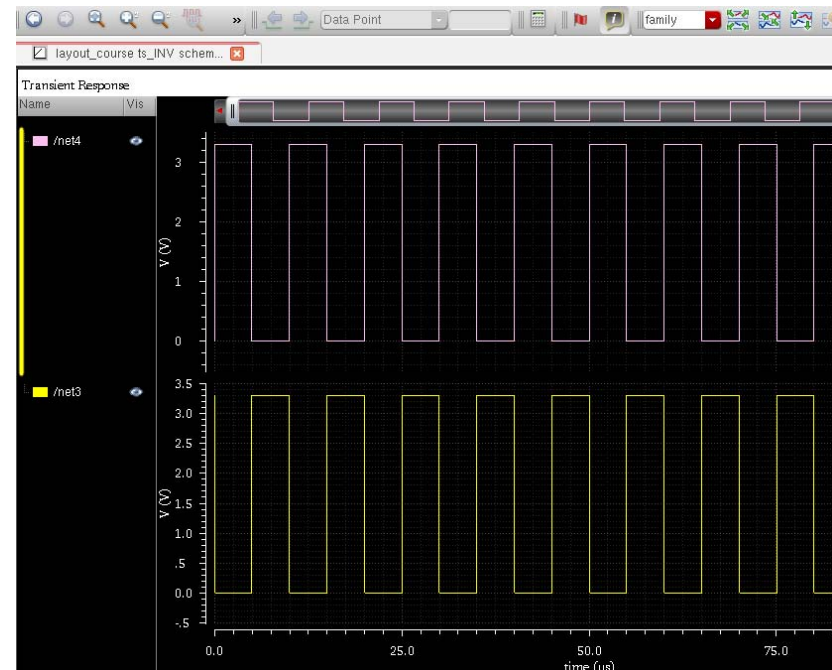
Pre-Simulation(cont'd)

- Run the simulation



Pre-Simulation(cont'd)

- Seperate and merge waveform



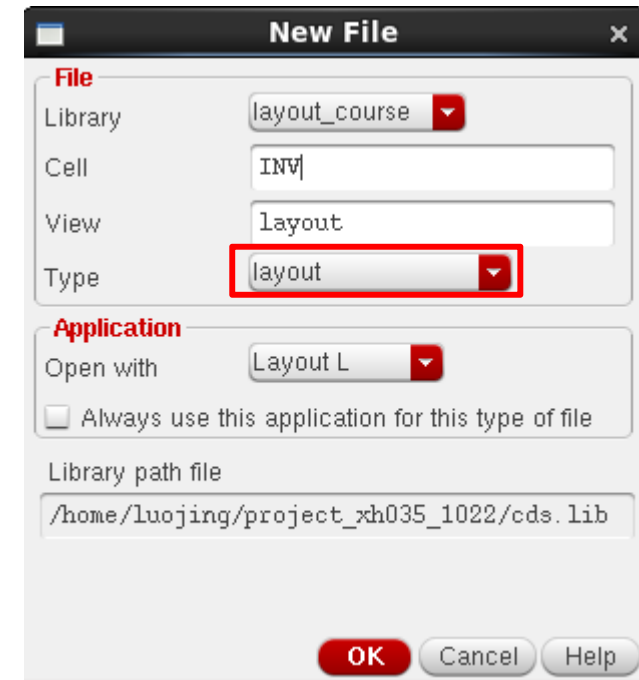
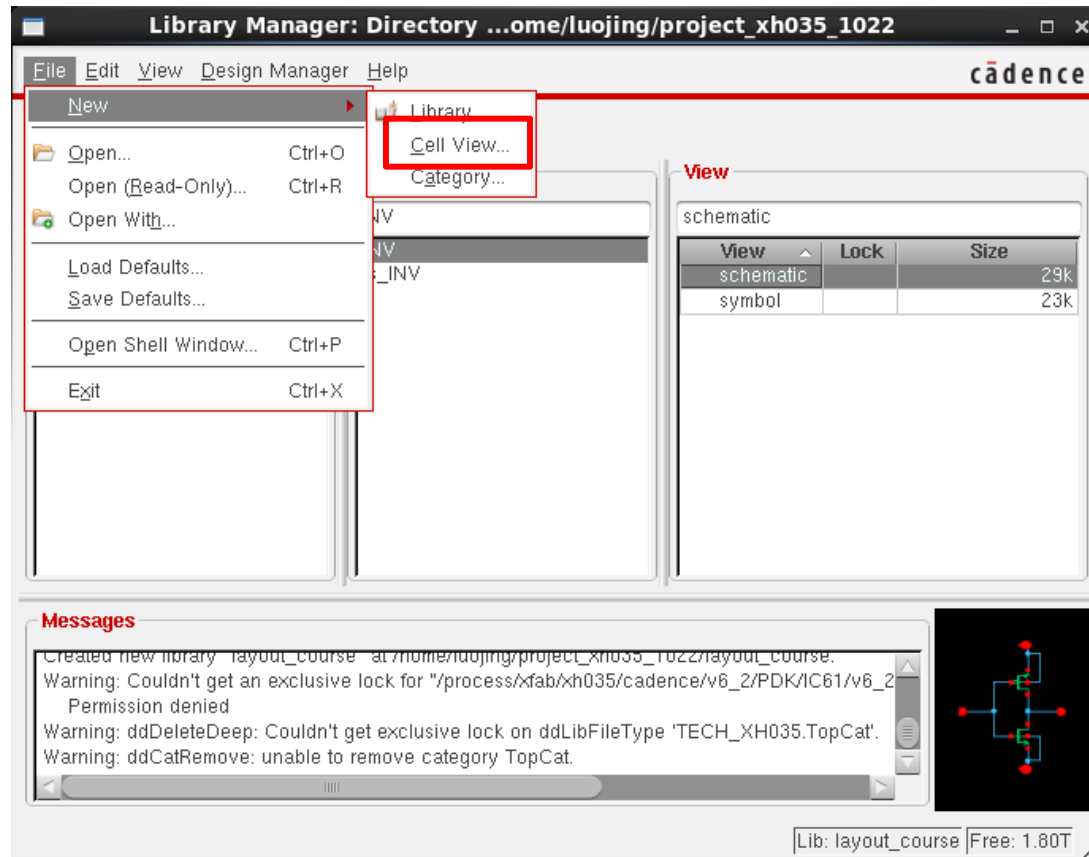
Pre-Simulation(cont'd)

- Zoom in or zoom out waveform



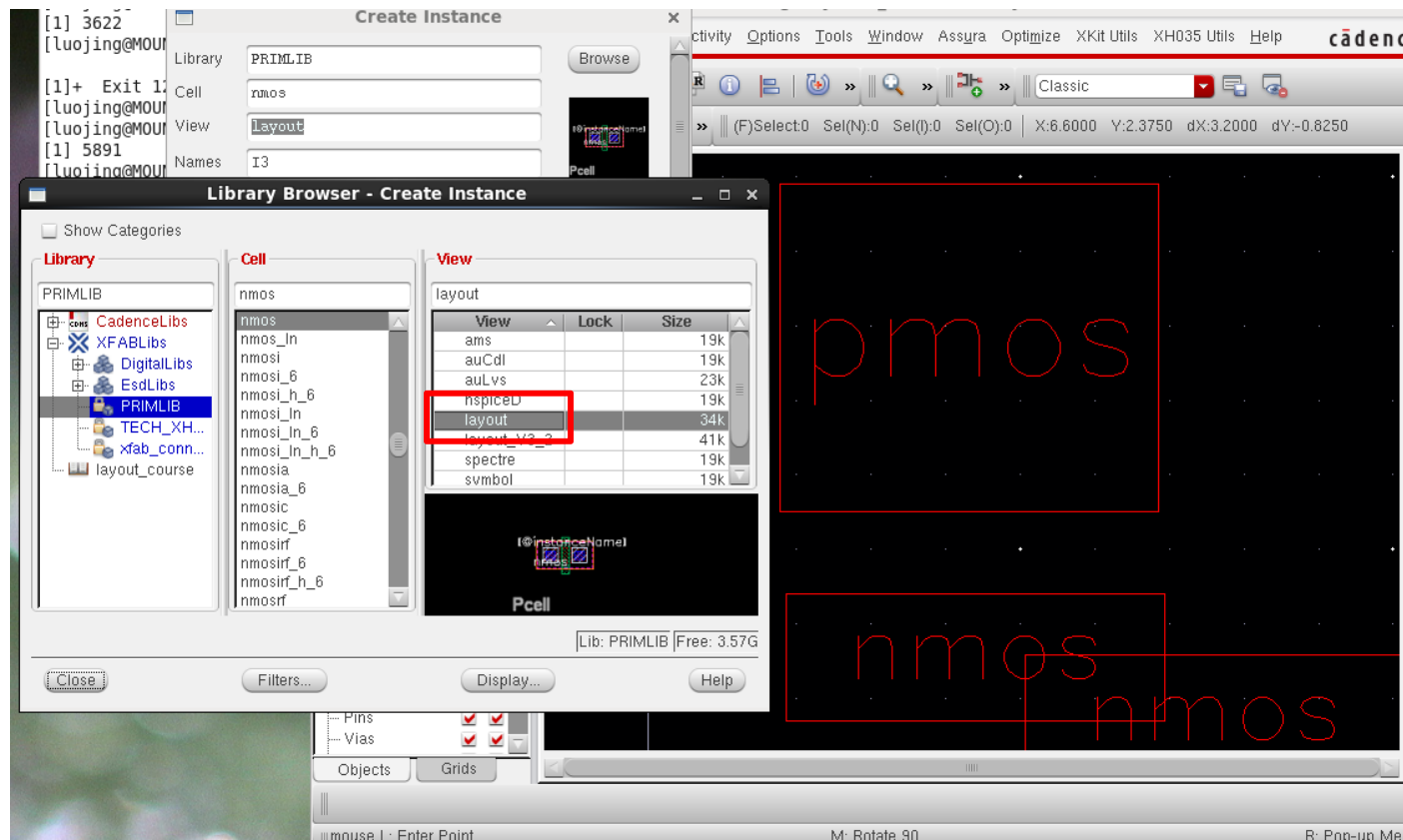
Layout design

■ Create a layout file



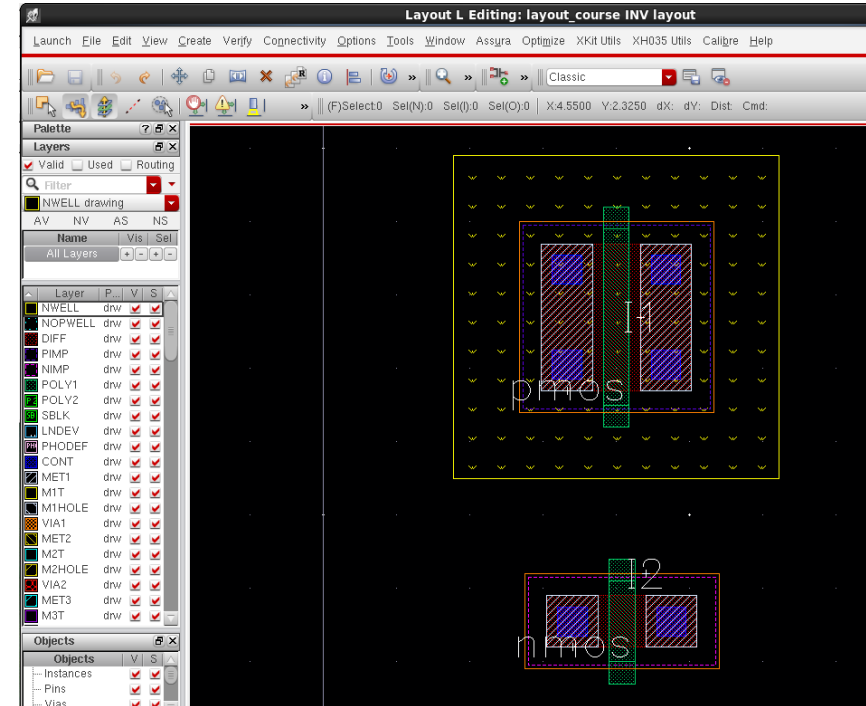
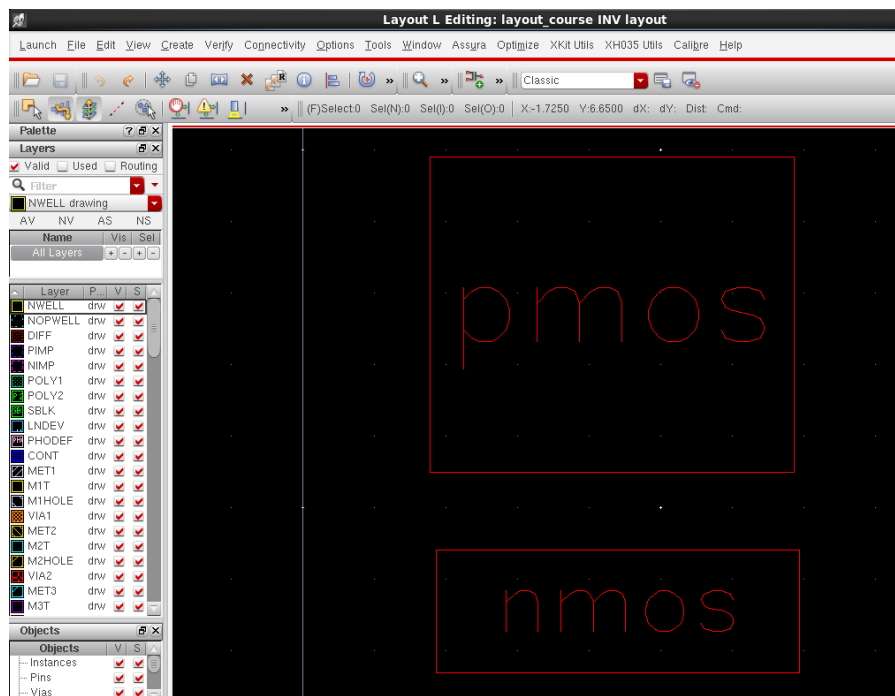
Layout design

- Add instances (manually, using shortcut— i)



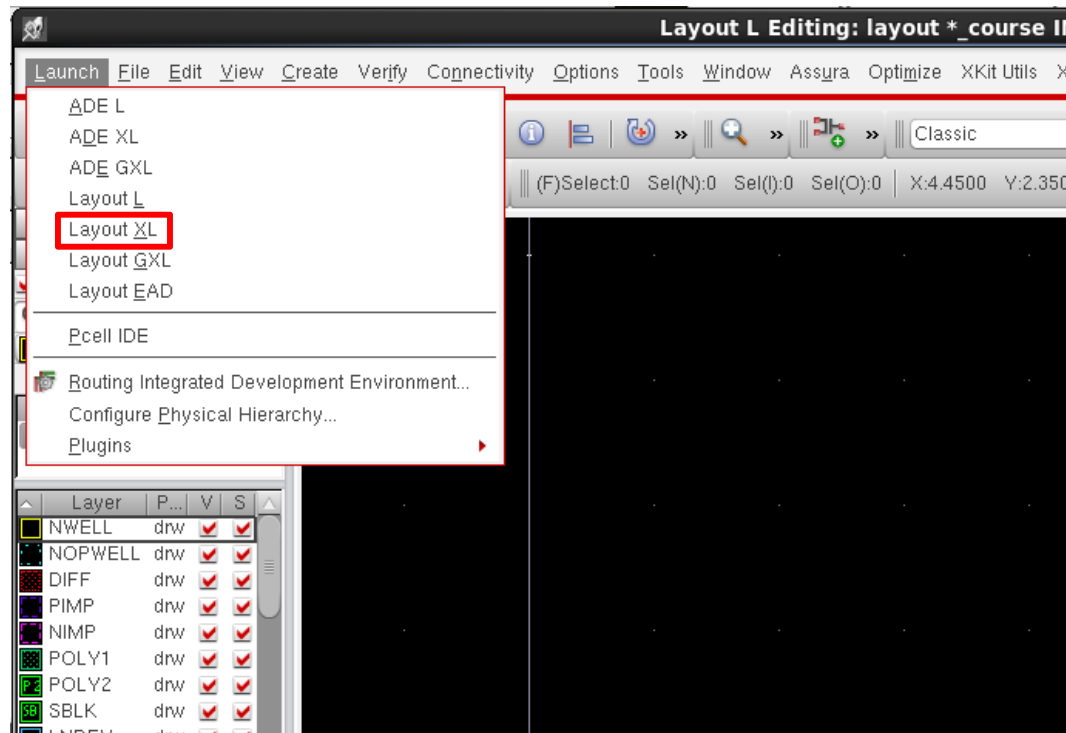
Layout design

- Display the layout of device(Shift + f)



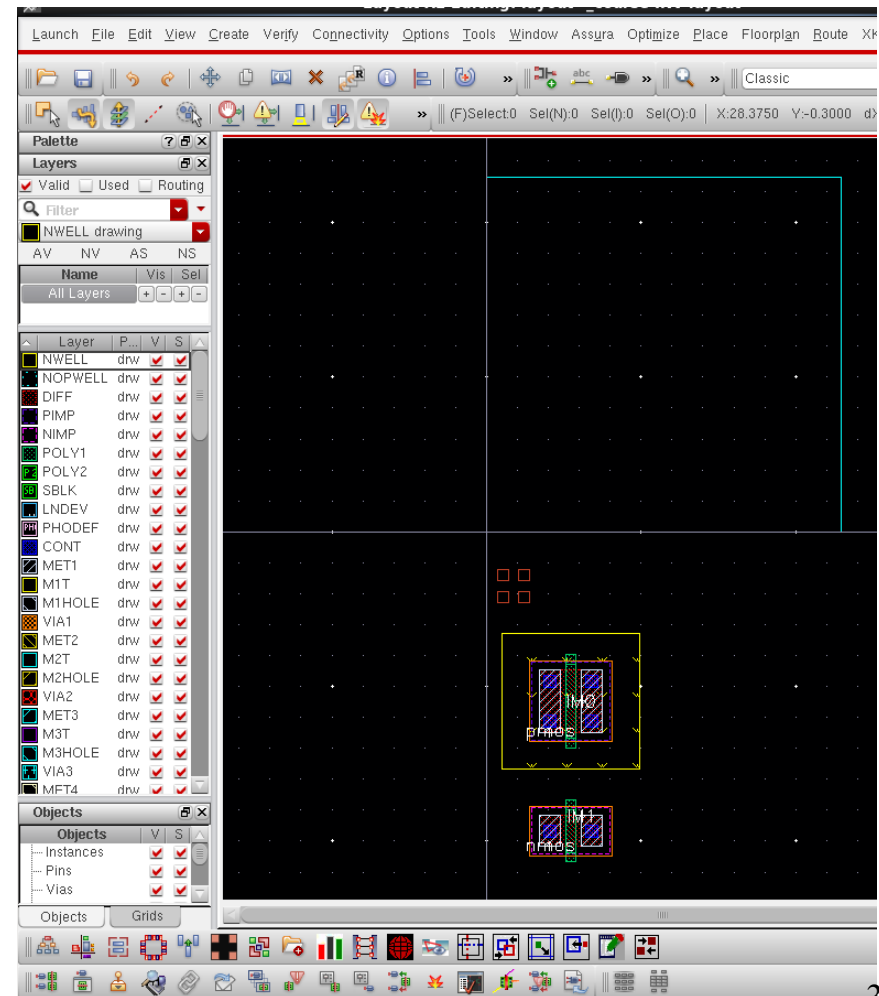
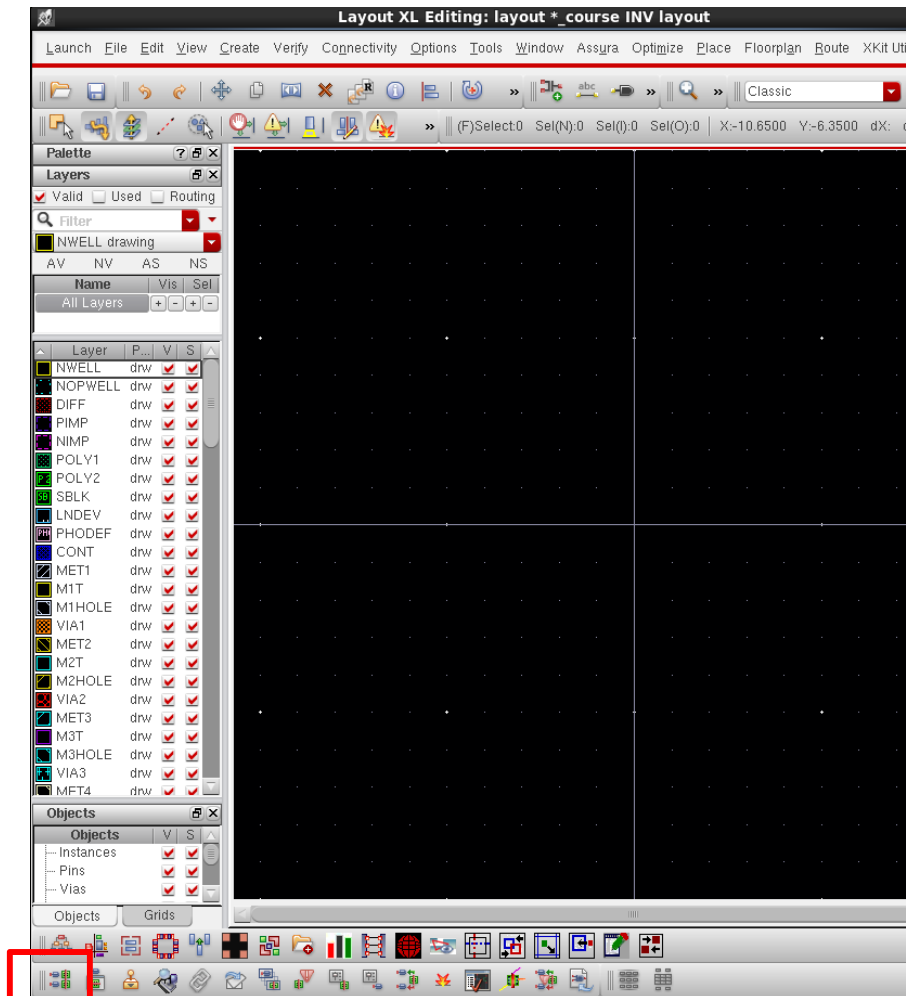
Layout design

- Another way to add instances (auto-generation)



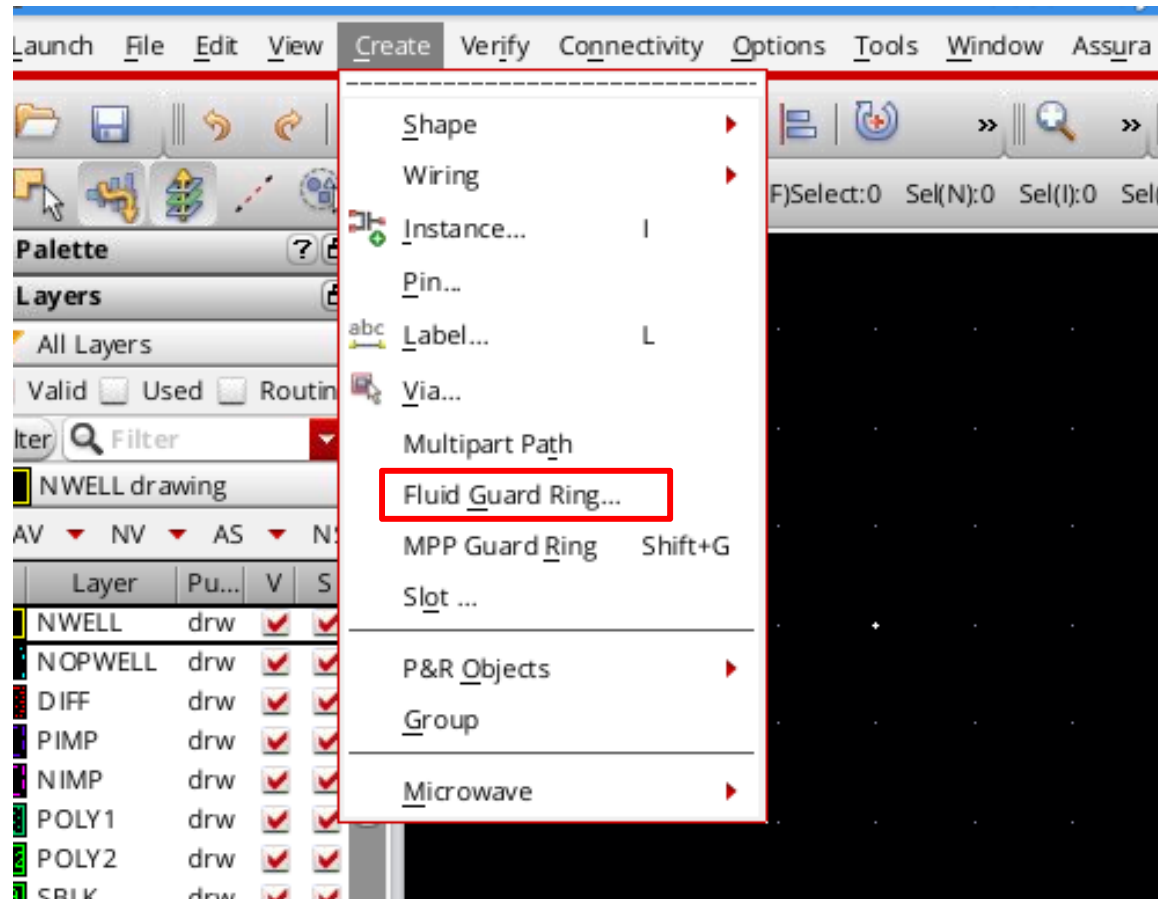
Layout design

- Click button to generate all from source



Layout design

■ Add VDD and GND contact



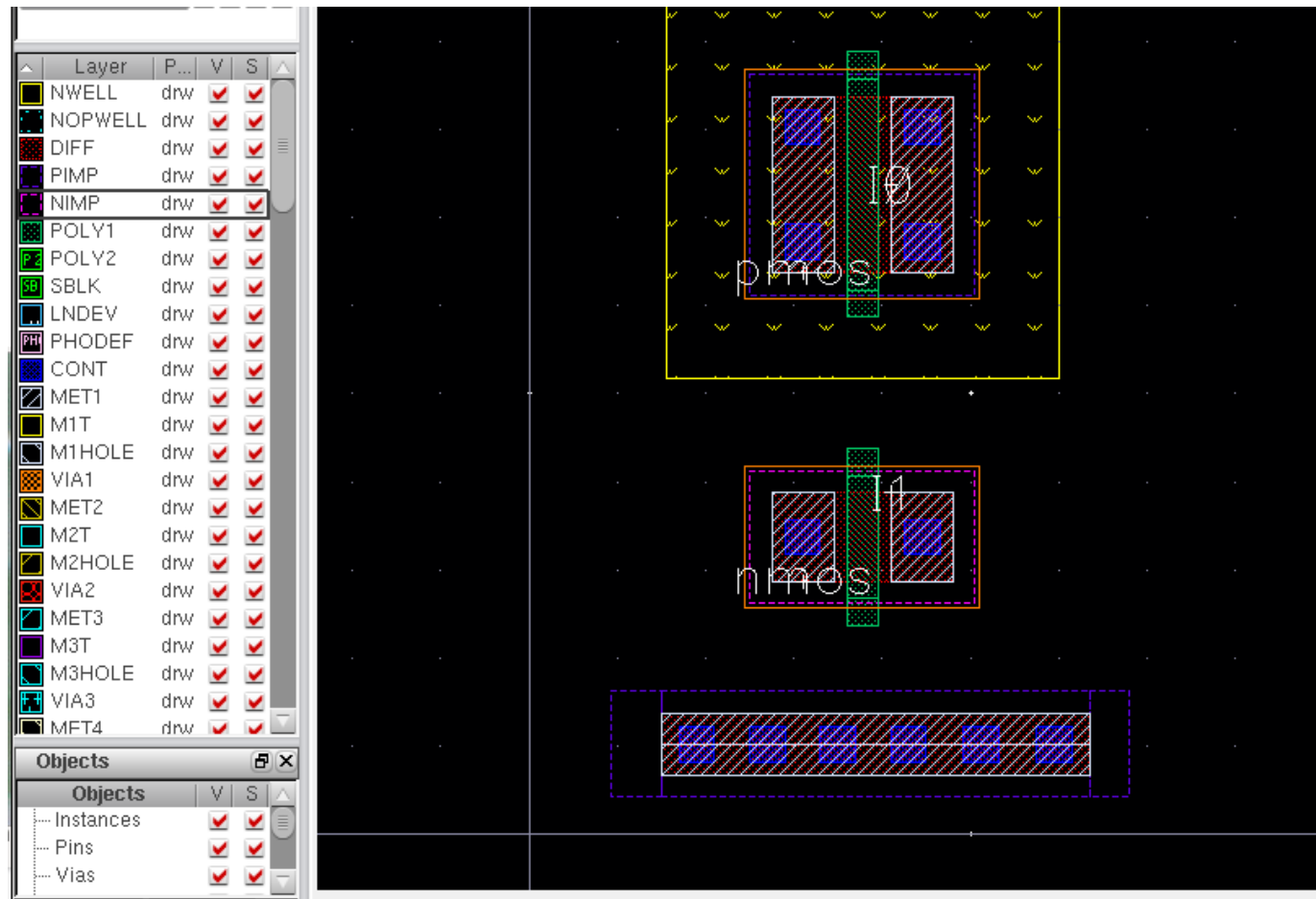
Layout design

- Choose Nguardring for VDD



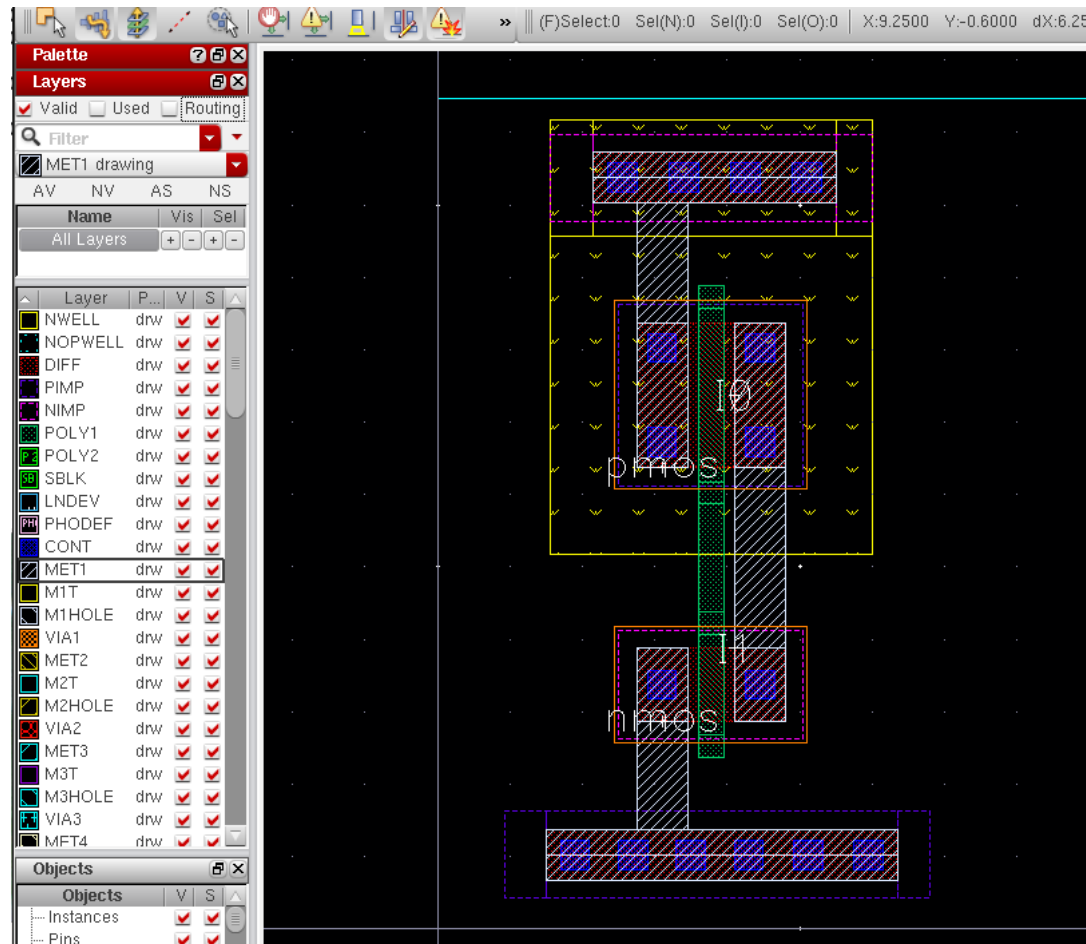
Layout design

- Choose Pguardring for GND



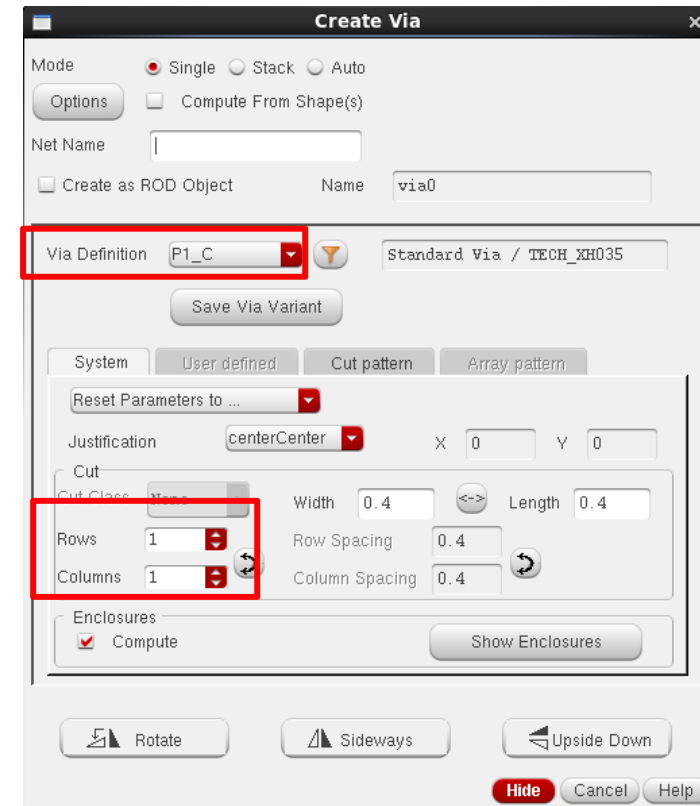
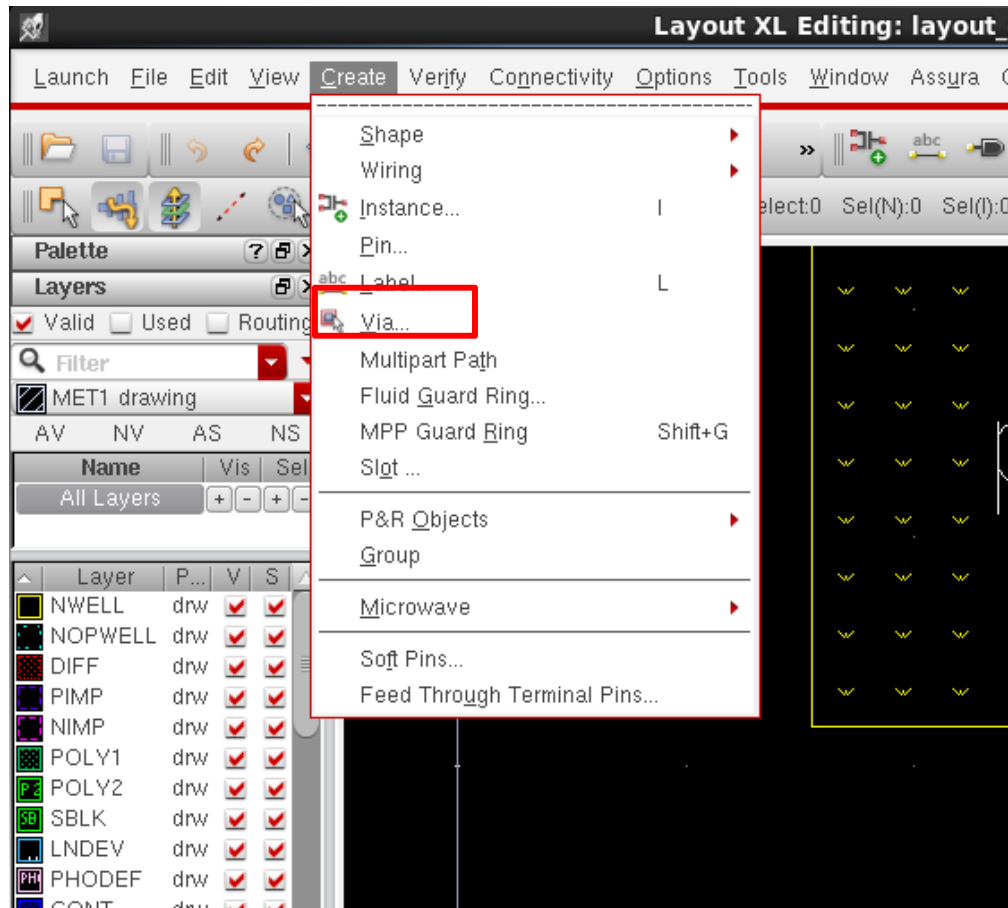
Layout design

- Add other path (shortcut key — p or r)



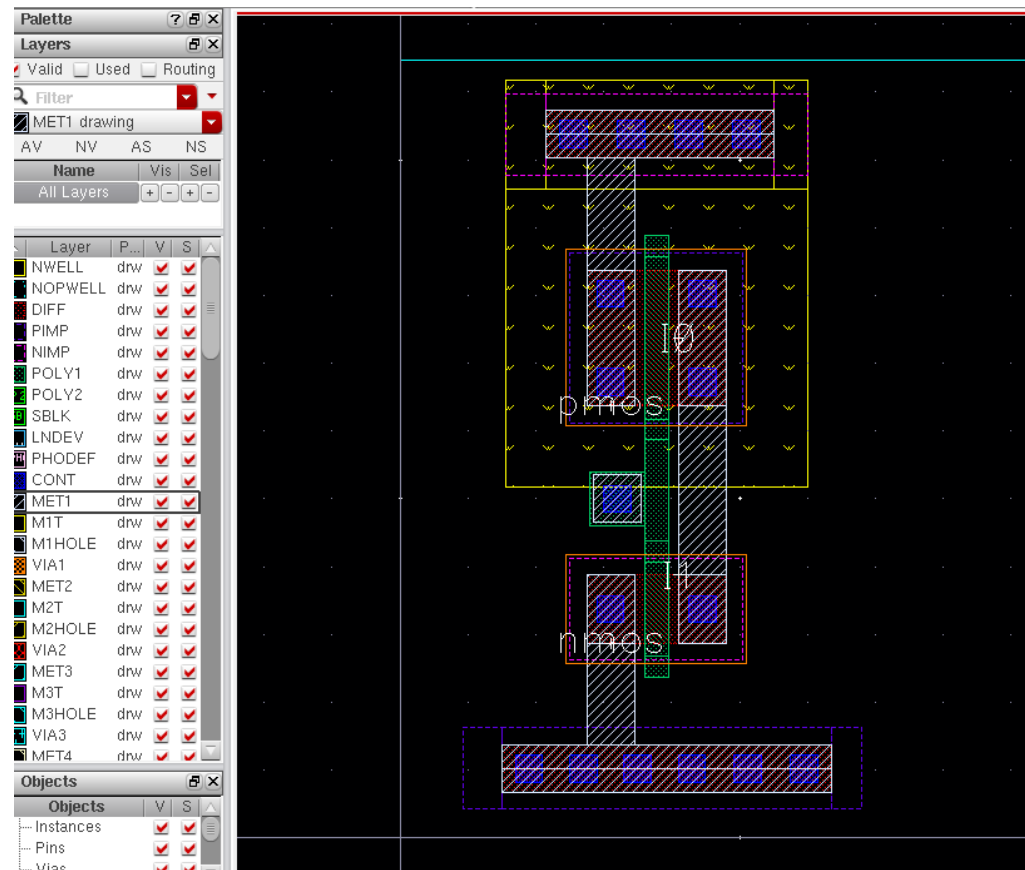
Layout design

■ Add via



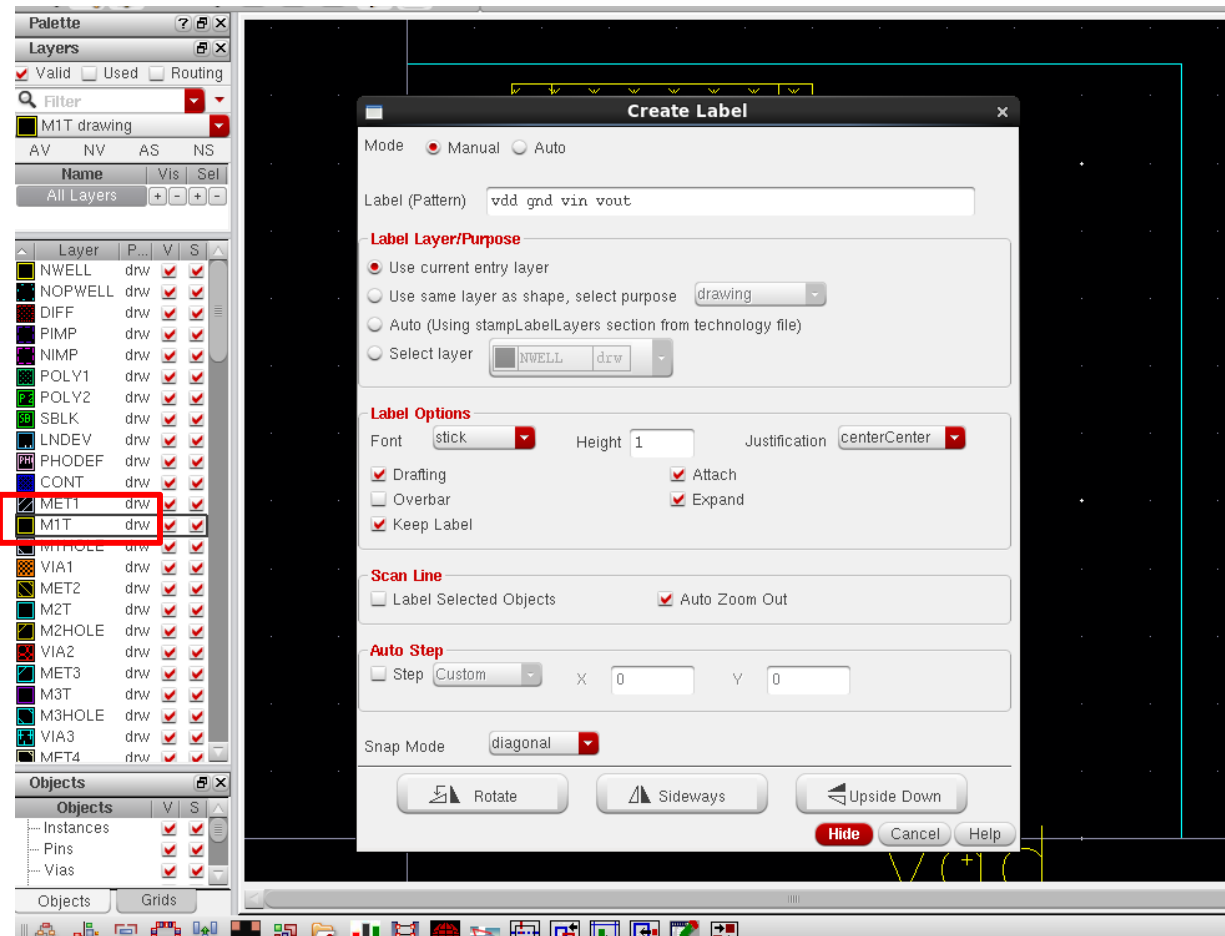
Layout design

- Add a via between poly and metal1



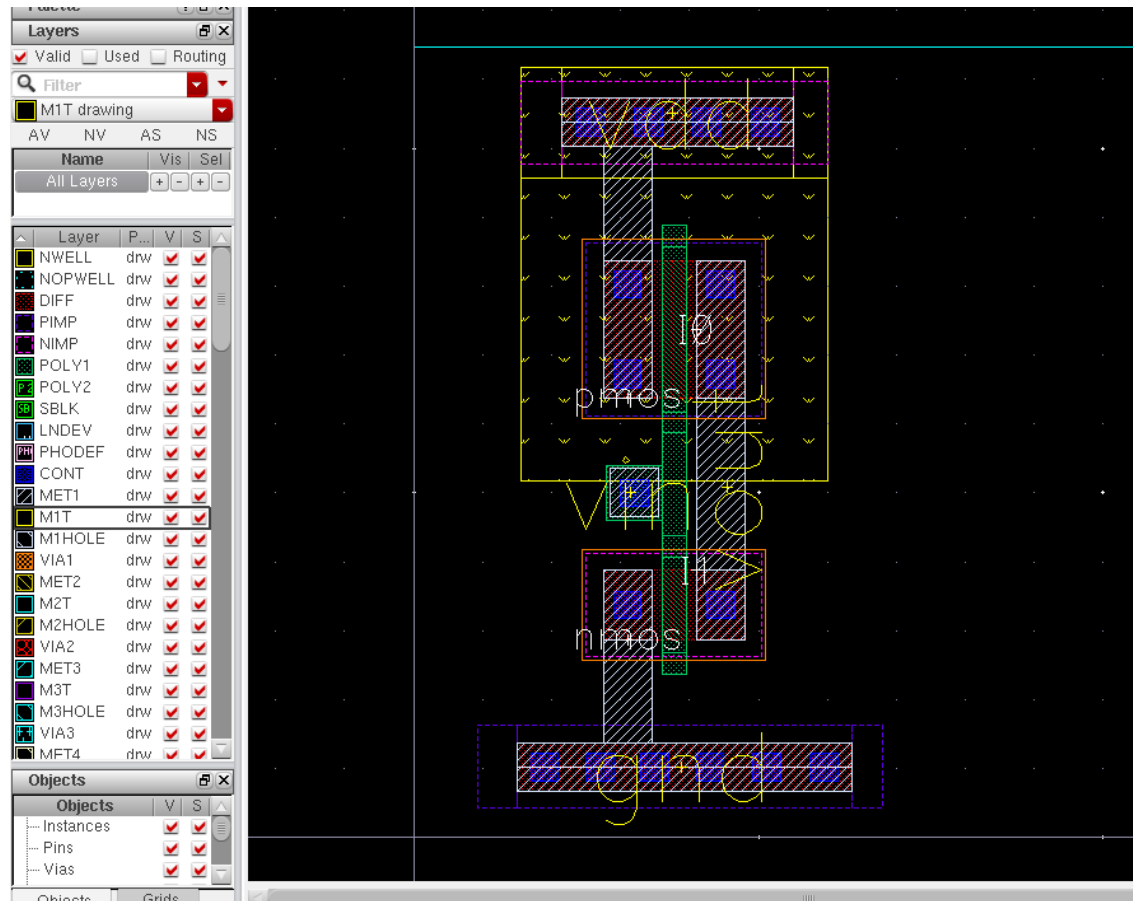
Layout design

- Add pin labels(shortcut key — 1)



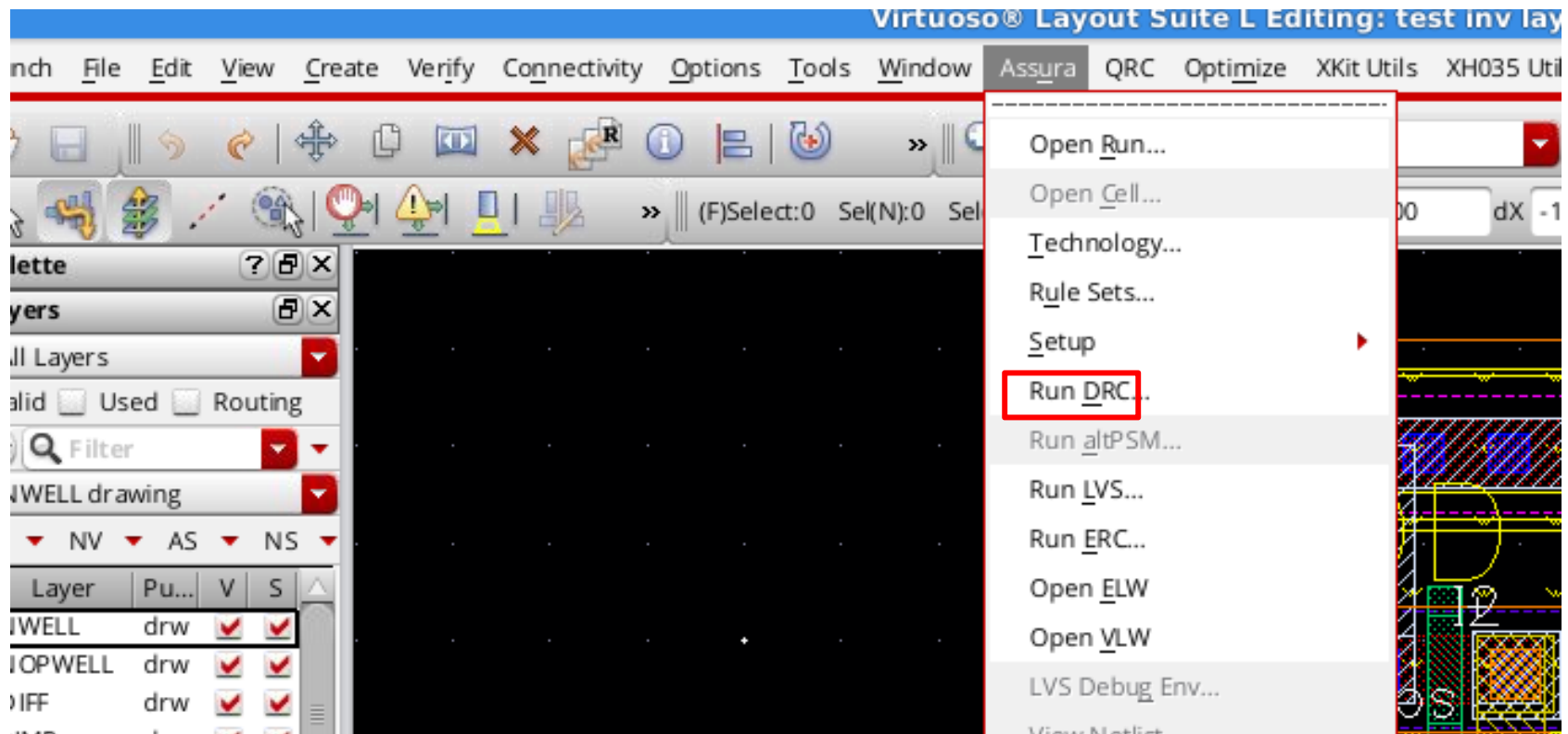
Layout design

- Add pins of vdd gnd vin vout



Layout design

■ Run DRC(design rule check)



Layout design

■ Run DRC

Run Assura DRC

Layout Design Source: DFI Compare two layouts: Generate LVL Compare Rules...

Library: test Cell: inv View: layout Browse...

Save Extracted View: View Name: drc_extracted

Area To Be Checked: Full

Run Name: inv_DRC Run Directory: ./AssuraDRC

Run Location: local

View Rules Files: Technology: XH035_1022 Rule Set: default

Rules File: v6_4/assura/v6_4_1/Assura/XH035_1022/drc.ru1 View... Reload

Switch Names: Set Switches

RSF Include: v6_4/assura/v6_4_1/Assura/XH035_1022/DRCinclude.rsf View...

Variable	Value	Default	Description
None			

View avParameters: Modify avParameters... 1 avParameter is set.

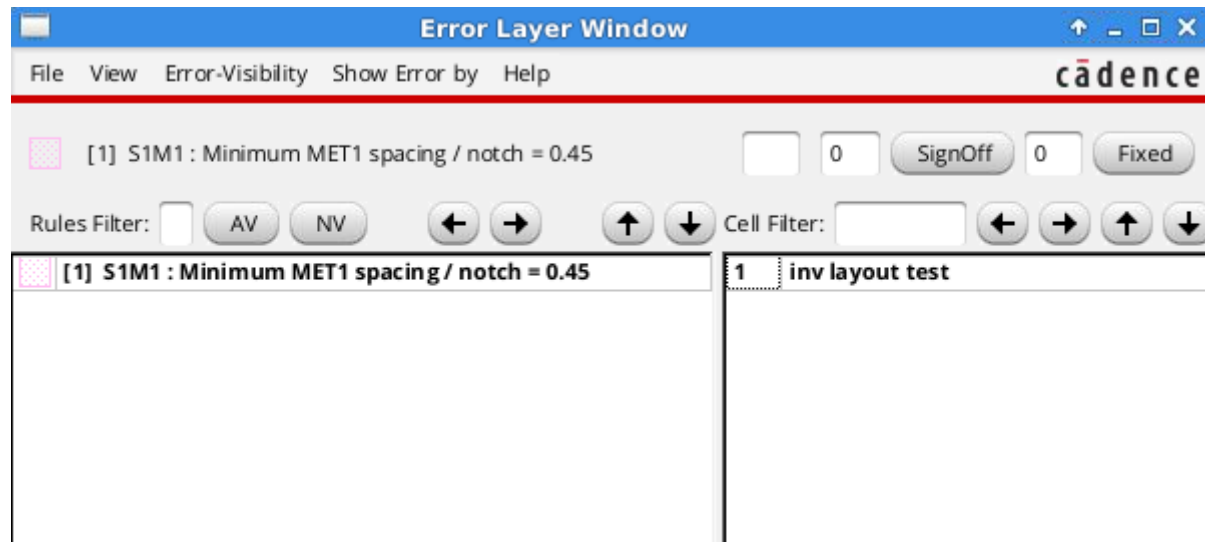
View Additional Functions: No additional functions are set.

Enable limitDrcCheck:

OK Cancel Apply Defaults Load State Save State View RSF Help

Layout design

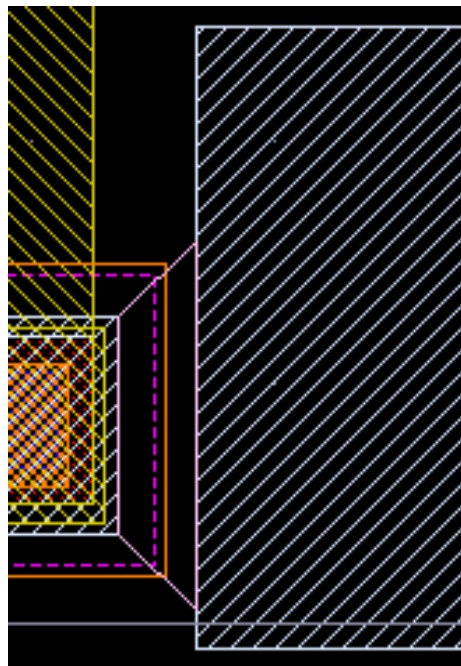
■ DRC results



- If you have DRC error, you can double click the error to highlight it in layout

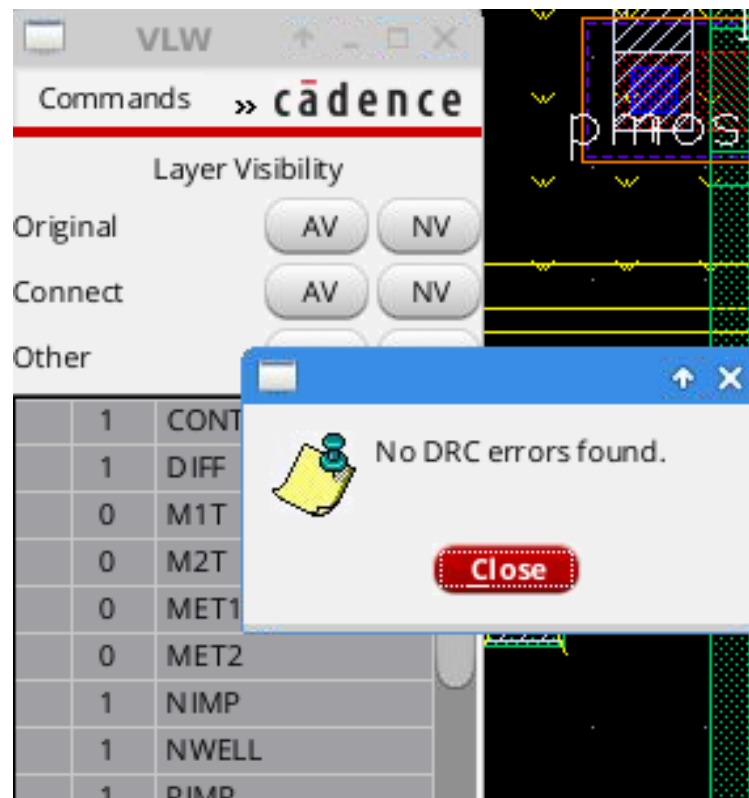
Layout design

- For example, this error means the distance between the MET1 is too close



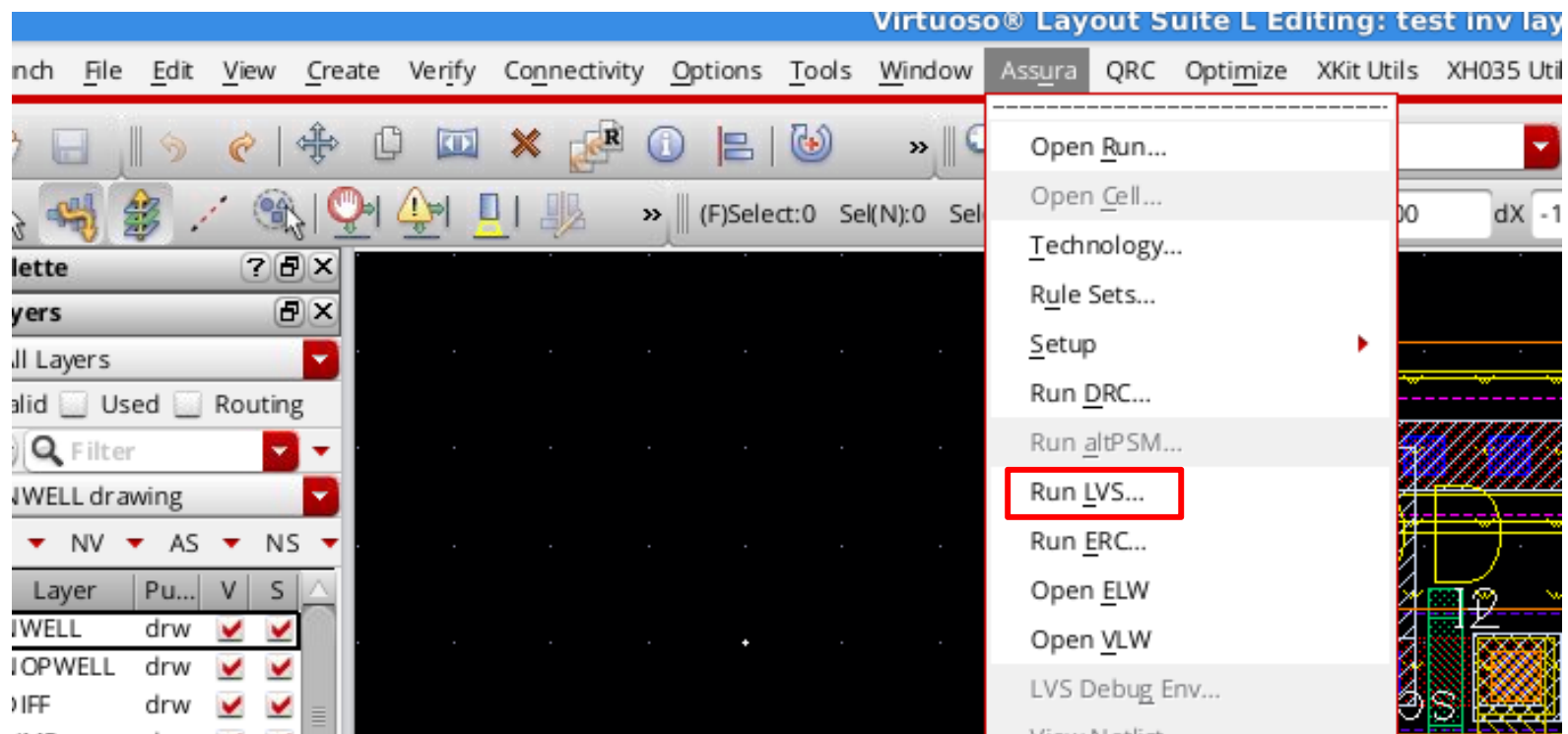
Layout design

- Finally, we need to ensure no DRC error



Layout design

■ Run LVS(layout VS schematic)



Layout design

■ Run LVS

Run Assura LVS

Schematic Design Source: DFI Use Existing Netlist Netlisting Options...
Use Verilog Top Cell

Library: test Cell: inv View: schematic Browse...

Layout Design Source: DFI Use Existing Extracted Netlist

Library: test Cell: inv View: layout Browse...

Run Name: inv_LVS Run Directory: ./AssuraLVS

Run Location: local

View Rules Files: Technology: XH035_1022 Rule Set: default

Extract Rules: /assura/v6_4_1/Assura/XH035_1022/extract.ru1 View... Reload

Compare Rules: g/project_xh035_1022/.assuraSetup/Assura/compare.inc View...

Switch Names: Set Switches

Binding File(s): View...

RSF Include: /v6_4/assura/v6_4_1/Assura/XH035_1022/LVSinclude.rsf View...

Variable	Value	Default	Description
None			

View avParameters: Modify avParameters... 1 avParameter is set.

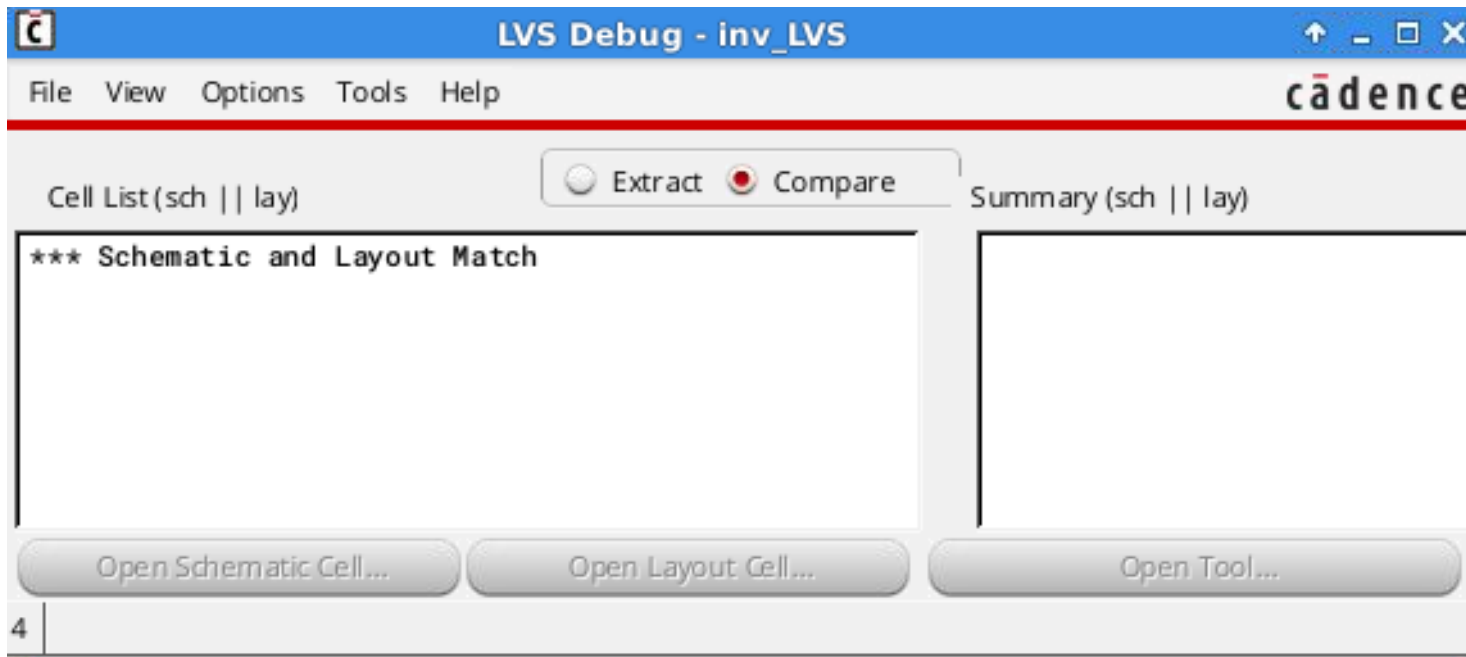
View avCompareRules: Modify avCompareRules... 4 avCompare rules are set.

View Additional Functions: No additional functions are set.

OK Cancel Apply Defaults Load State Save State View RSF Help

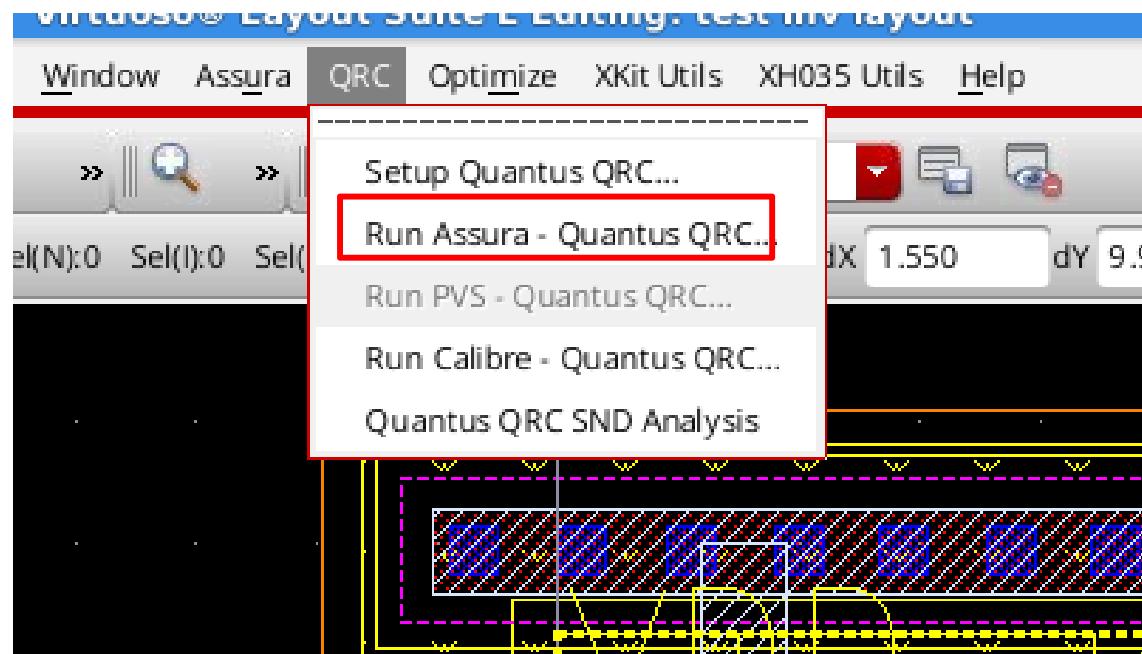
Layout design

- Finally, we have to get this Match result



Post-Simulation

■ Run QRC



Post-Simulation

■ Run QRC

The screenshot shows the 'Quantus QRC (Assura) Parasitic Extraction Run Form' dialog box. It has a blue title bar and a tabbed interface with 'Setup', 'Extraction', 'Filtering', 'Netlisting', 'Run Details', and 'Substrate' tabs. The 'Setup' tab is active. The dialog contains several sections for file selection and parameter configuration.

File Selection Section:

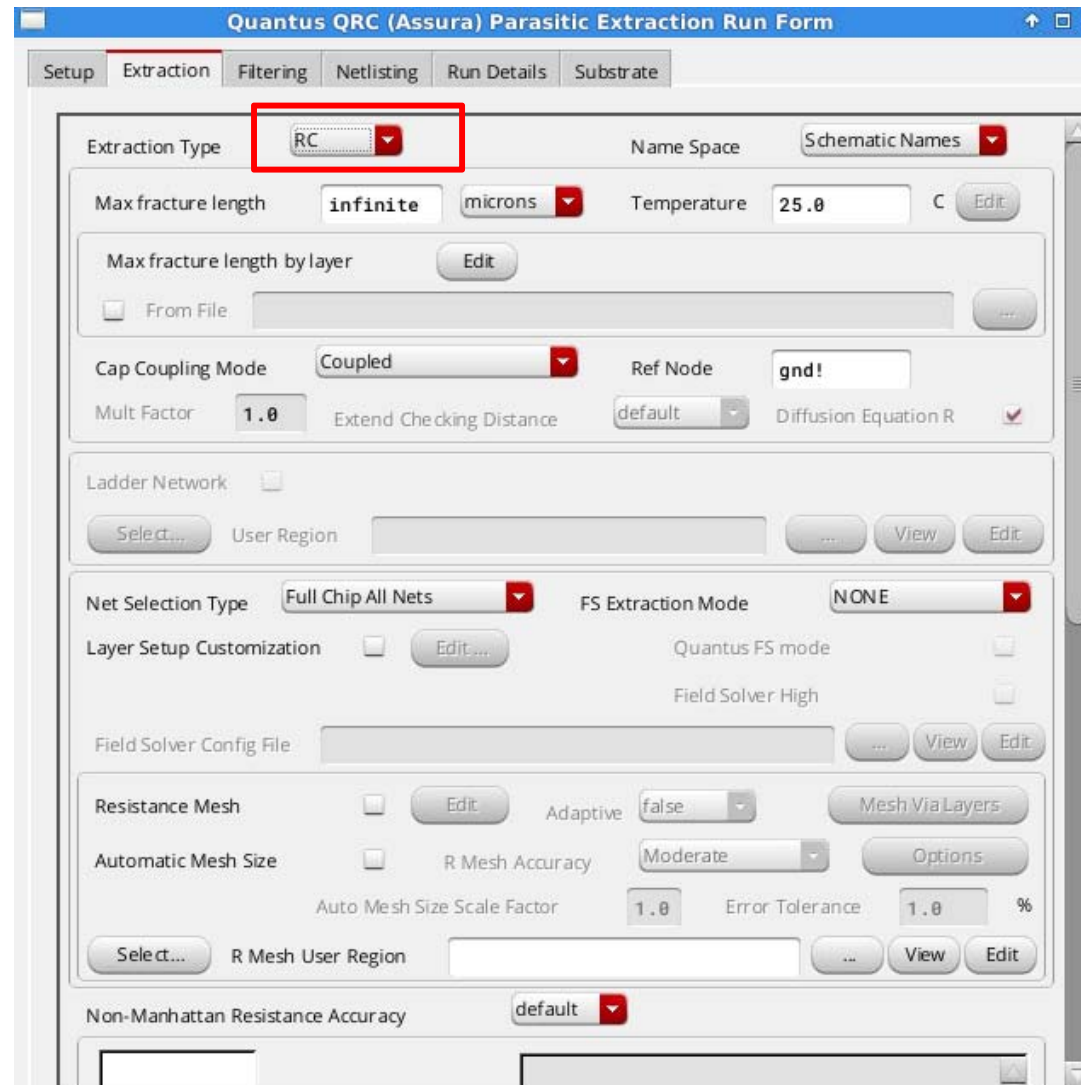
- Setup Dir: `f:\xkit\setup\XH035\cadence\QRC_assura\XH035_1022\QRC-Typ`
- Include Command File: [Empty]
- Rule Command File Include: [Empty]
- Tech Gnd File: User [Empty]
- Layer Setup File: [Empty]
- LPE Config File: [Empty]
- Library Cell Mapping File: [Empty]
- Library Definitions File: `/home/luojing/project_xh035_1022/cds.lib`
- Probe Text File: [Empty]

Configuration Section:

- Output: **Extracted View** (checked), Lib: `test`, Cell: `inv`, View: `log_extracted`
- Enable CellView Check:
- Parasitic Res Component: `p_res auLvs PRIMLIB`, Prop Id: `r`
- Parasitic Cap Component: `p_cap auLvs PRIMLIB`, Prop Id: `c`
- Parasitic Ind Component: `pinductor`, Prop Id: `l`
- Parasitic M Component: `pmind`, Prop Id: `k`
- Inductance L1 Prop Id: `ind1`, Inductance L2 Prop Id: `ind2`
- Parasitic CCVS Component: `ccvs`, Hgain Prop Id: `hgain`, Vref Prop Id: `vref`
- Parasitic VS Component: `vsource`, Prod Id: `vr`
- Call Procedure: [Empty]

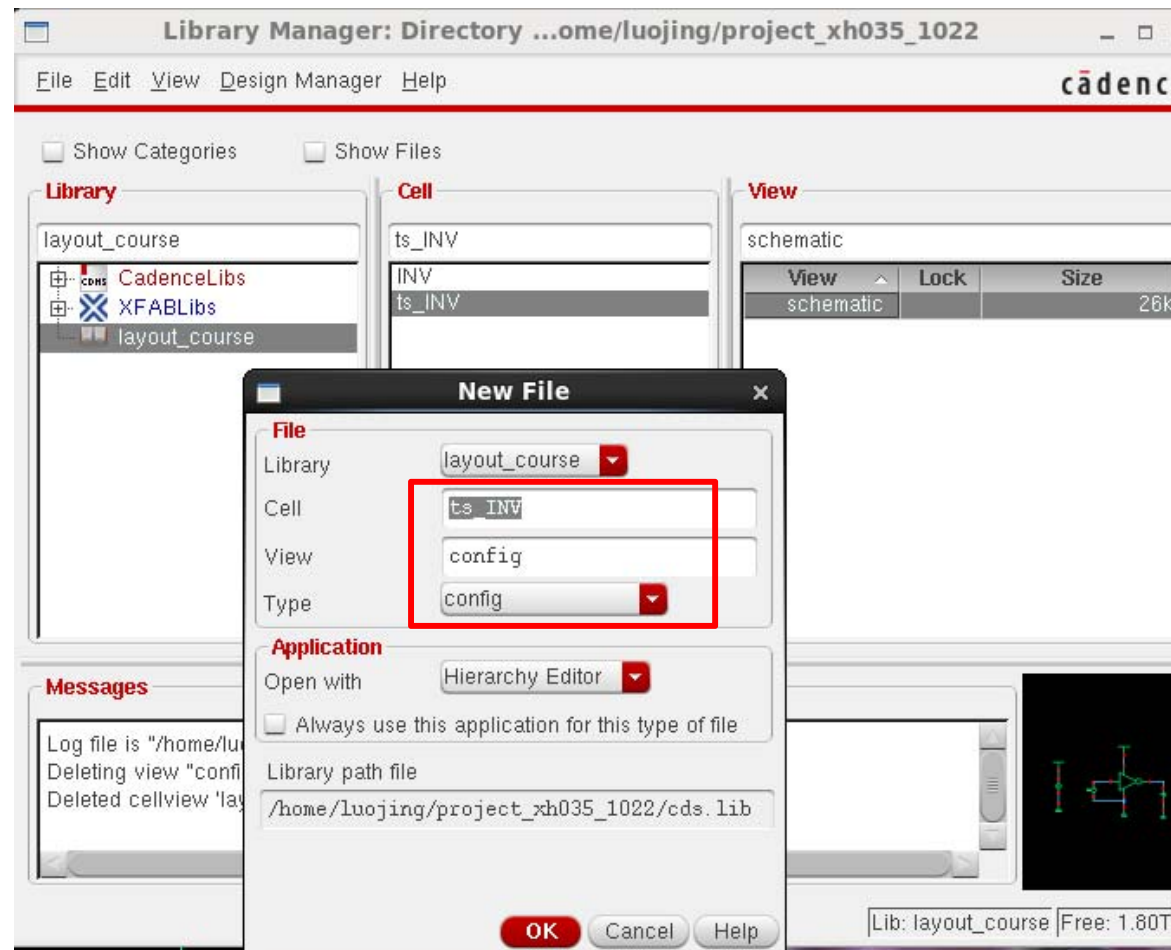
Post-Simulation

■ Run QRC



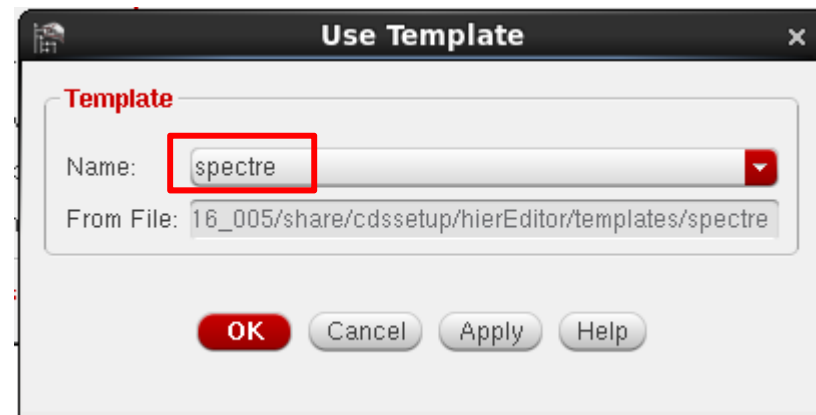
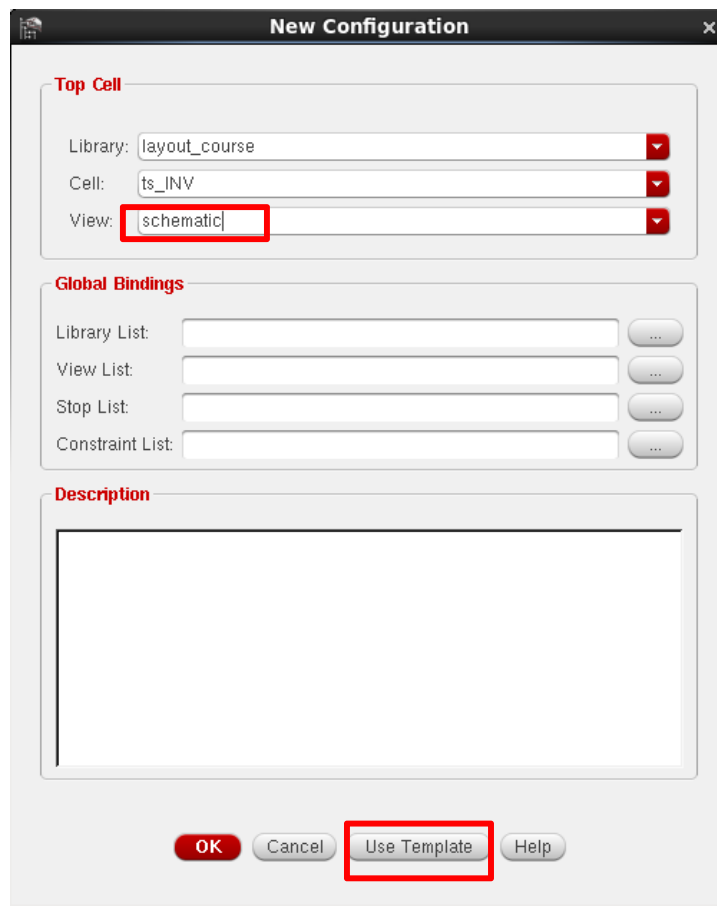
Post-Simulation

■ Create config file



Post-Simulation

■ Setup for config file



Post-Simulation

■ Setup for config file

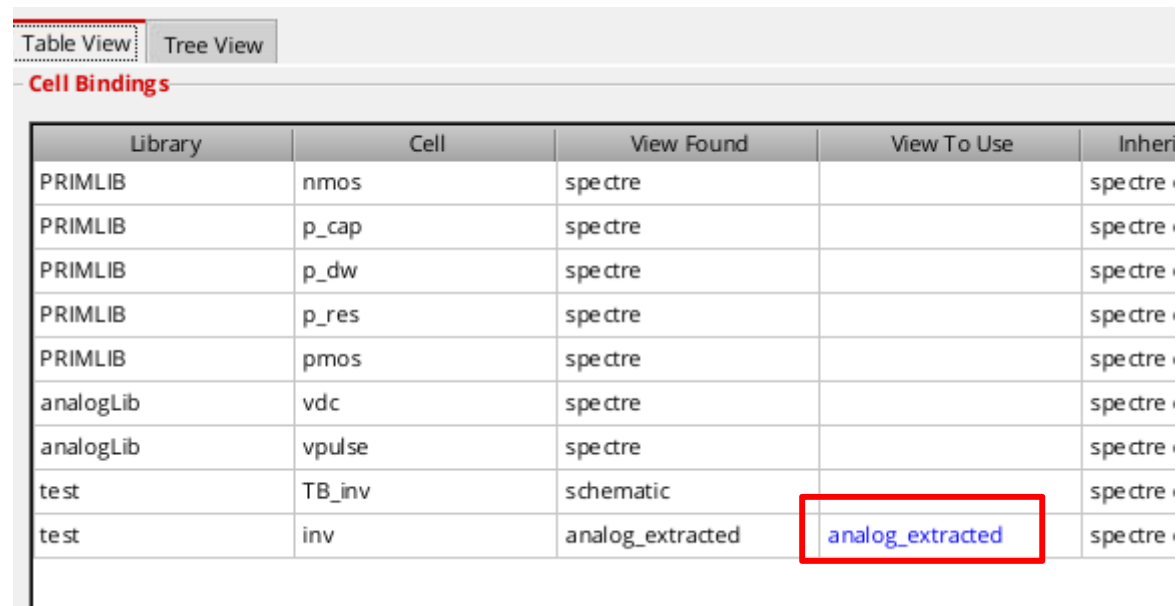


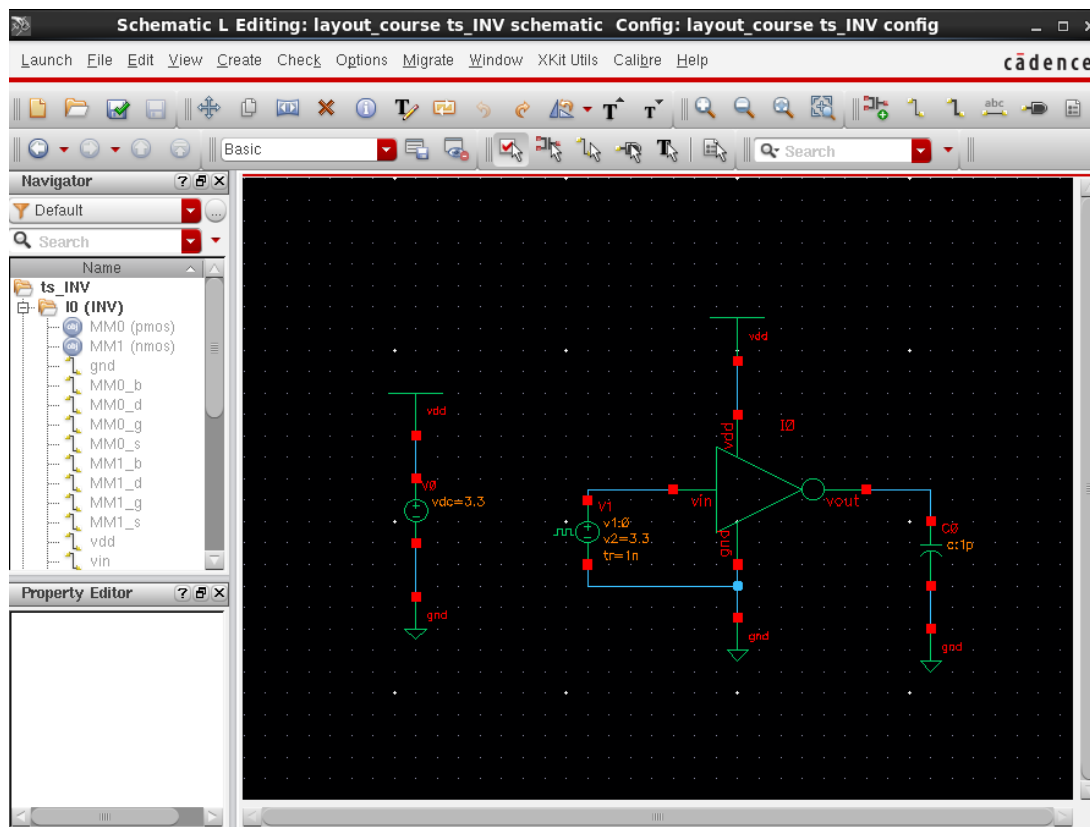
Table View Tree View

Cell Bindings

Library	Cell	View Found	View To Use	Inheri
PRIMLIB	nmos	spectre		spectre
PRIMLIB	p_cap	spectre		spectre
PRIMLIB	p_dw	spectre		spectre
PRIMLIB	p_res	spectre		spectre
PRIMLIB	pmos	spectre		spectre
analogLib	vdc	spectre		spectre
analogLib	vpulse	spectre		spectre
test	TB_inv	schematic		spectre
test	inv	analog_extracted	analog_extracted	spectre

Post-Simulation

■ Open config file



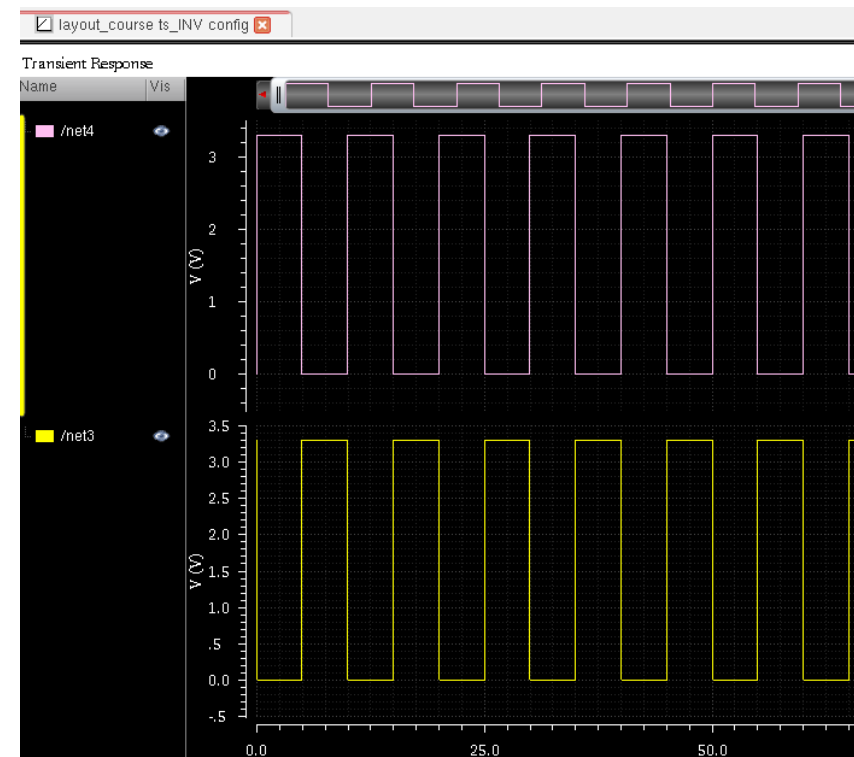
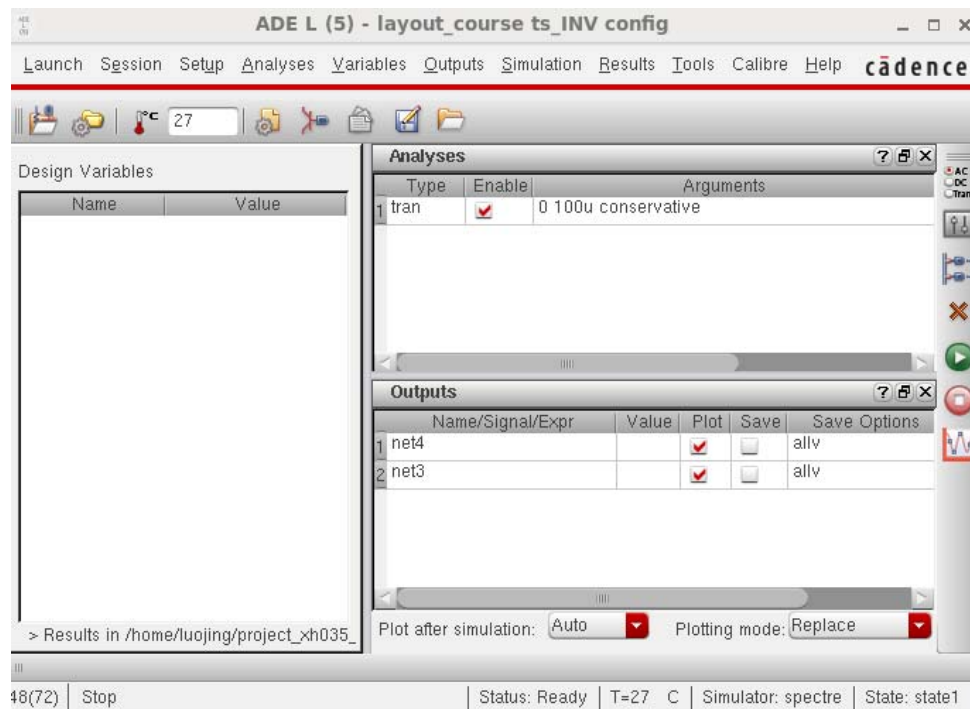
e — enter in sub-block

shift + b — retreat from

sub-block

Post-Simulation

- Run post-simulation, the same as pre-sim



Some shortcut keys

■ Some shortcut keys for layout

f — full screen display

k — ruler

Shift + k — clear ruler

m — move

c — copy

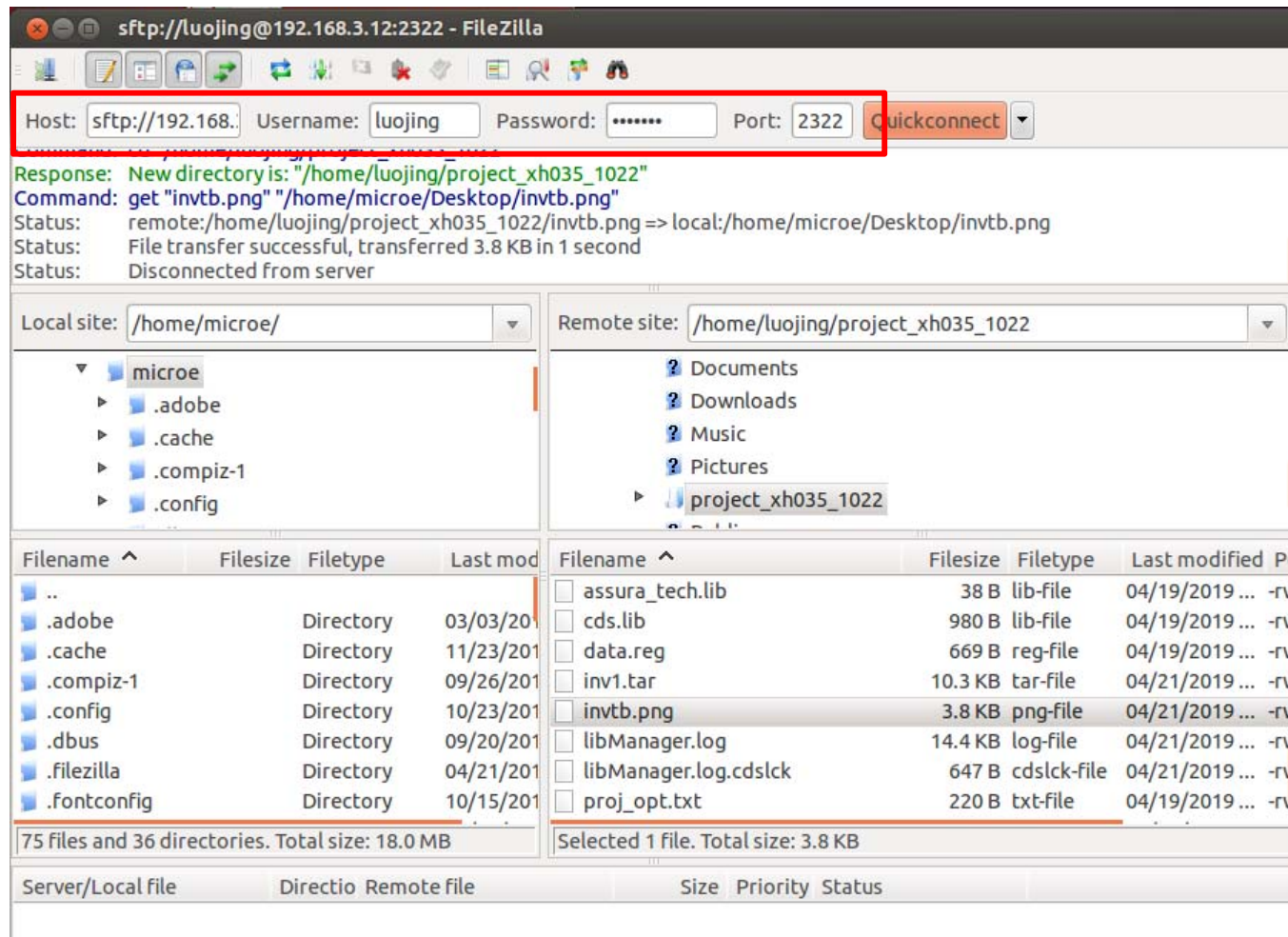
u — revoke

p — draw path

r — draw rectangle

FileZilla

- Use it to download your files





Thanks !