



上海交通大学
SHANGHAI JIAO TONG UNIVERSITY



Final project

Due: June 14th

电子版pdf格式发至邮箱: luojing@sjtu.edu.cn

纸质版上课时交给助教

Presentation at 14:00-15:40, June 14th

Outline

■ 3-bit 50MSPS SAR ADC

- Structure
- Your task

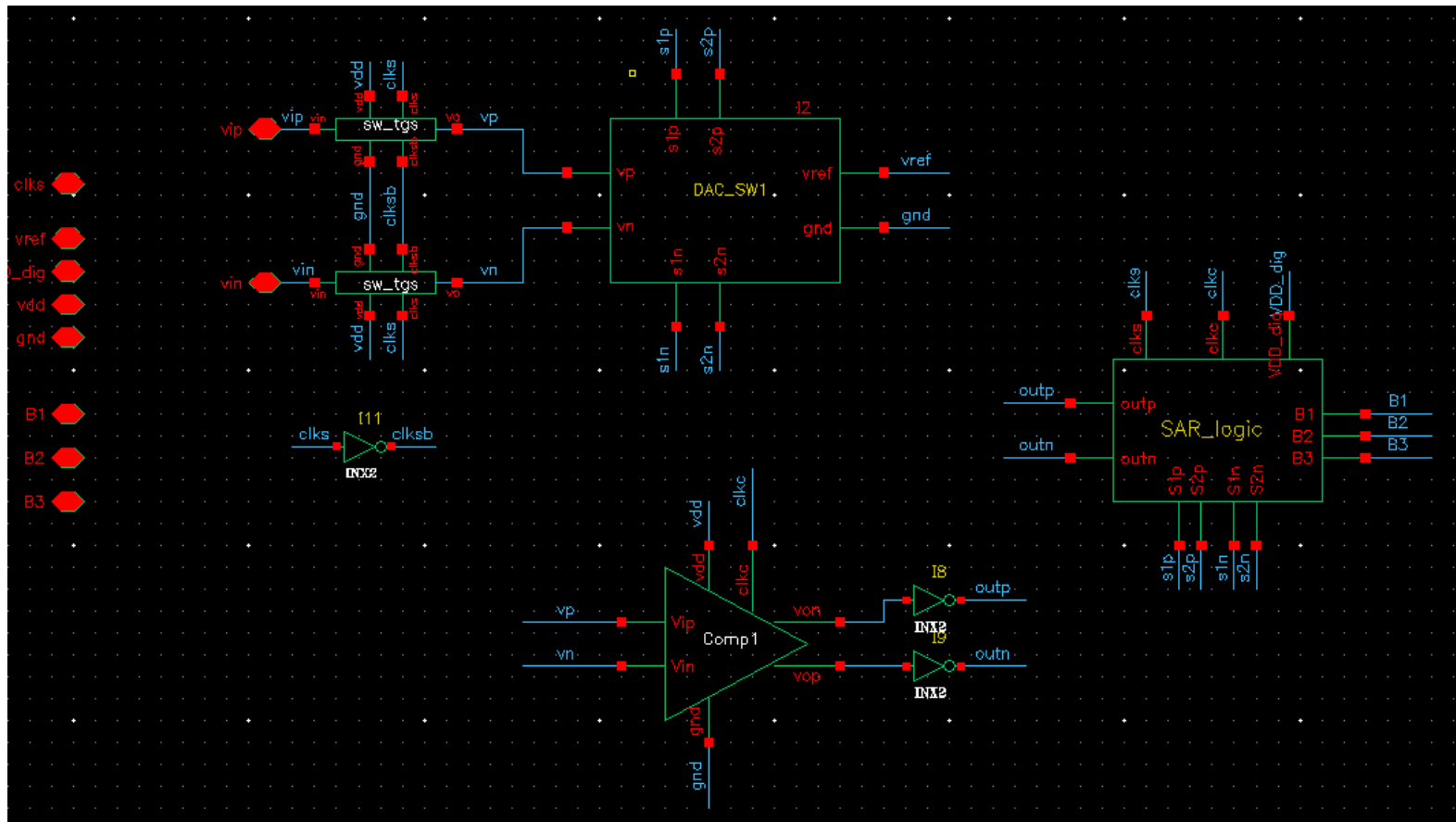
■ 2-stage OPA

- Structure
- Your task

■ Choose the one you want to do!

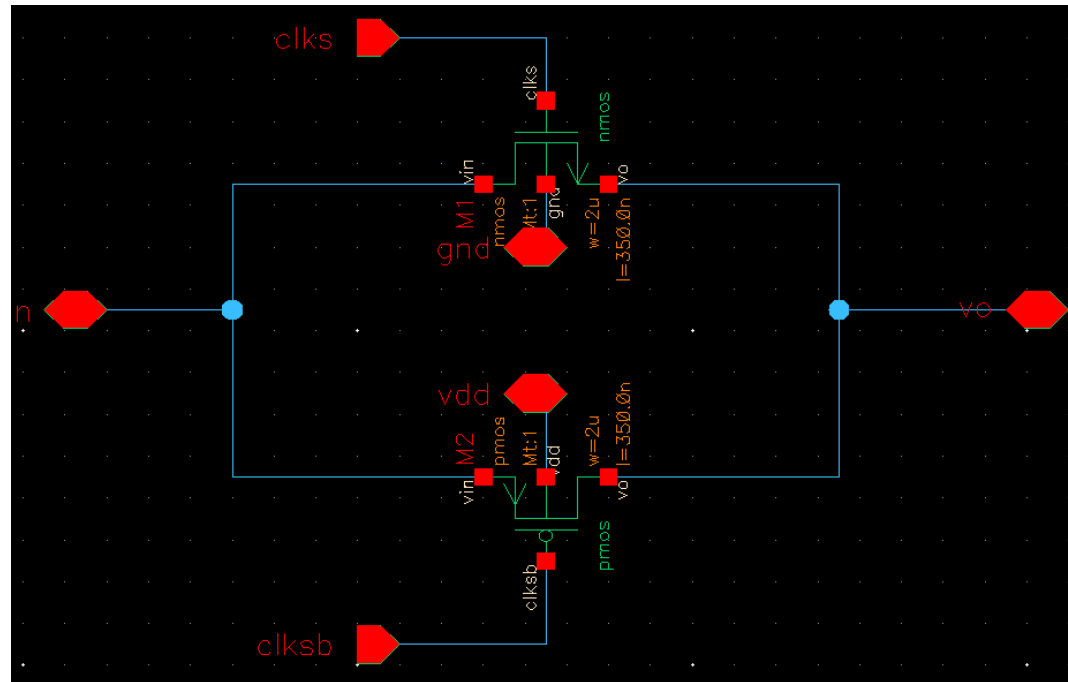
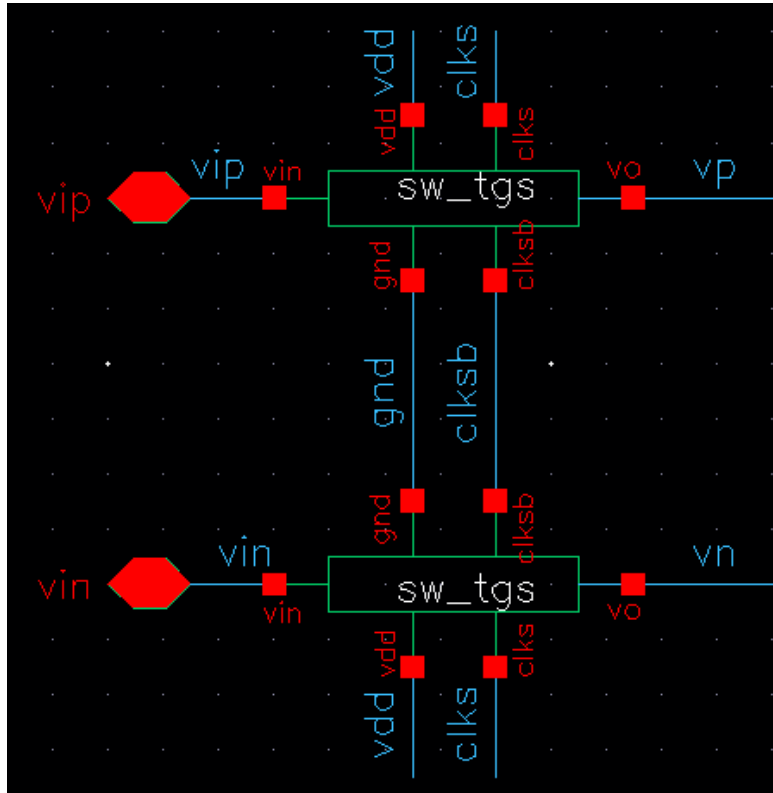
3-bit SAR ADC

- Structure of SAR ADC
- Sample and hold, Capacitive DAC, Comparator and SAR logic



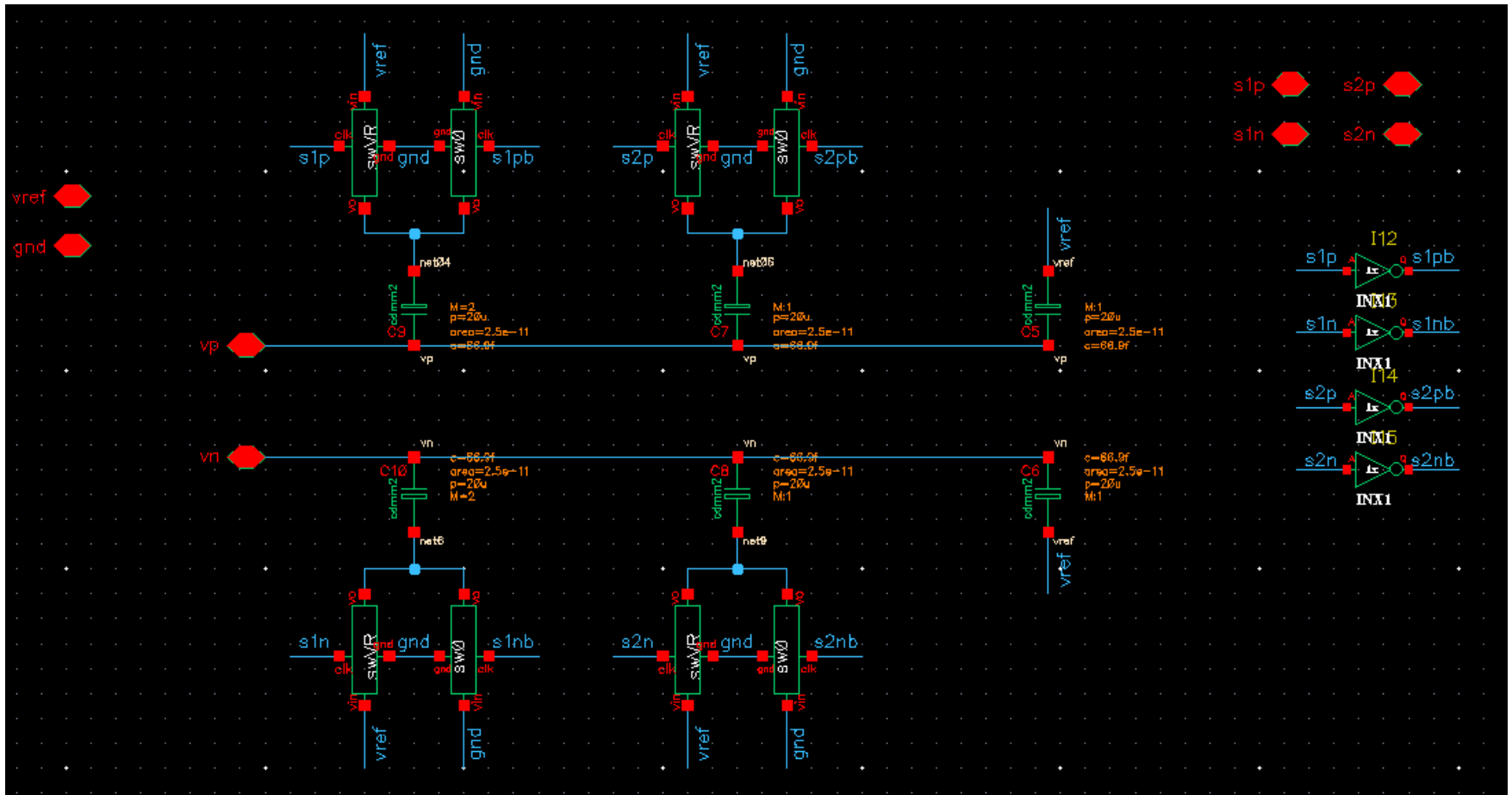
3-bit SAR ADC

- Sample and hold — transmission gate



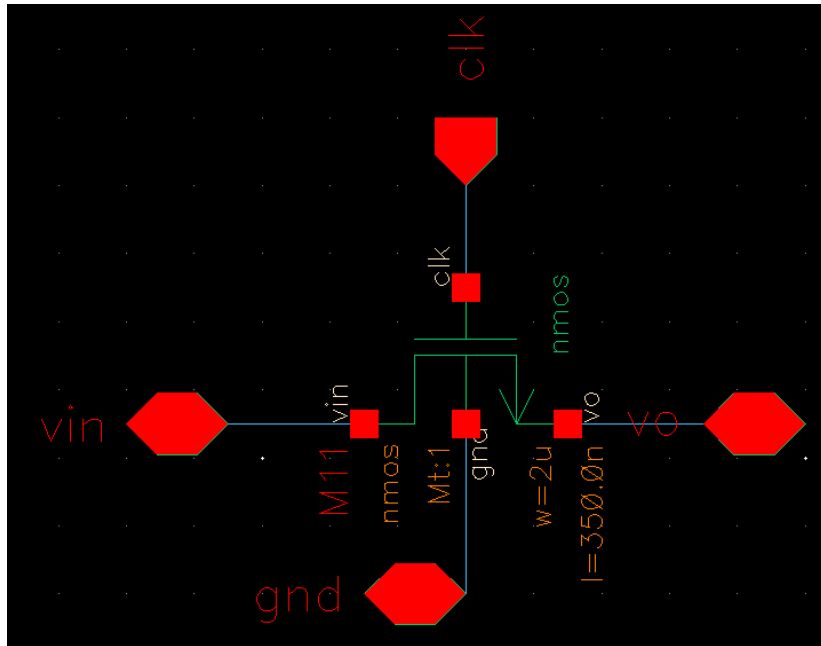
3-bit SAR ADC

- Capacitive DAC — unity cap 66.9fF, sw0, swVR

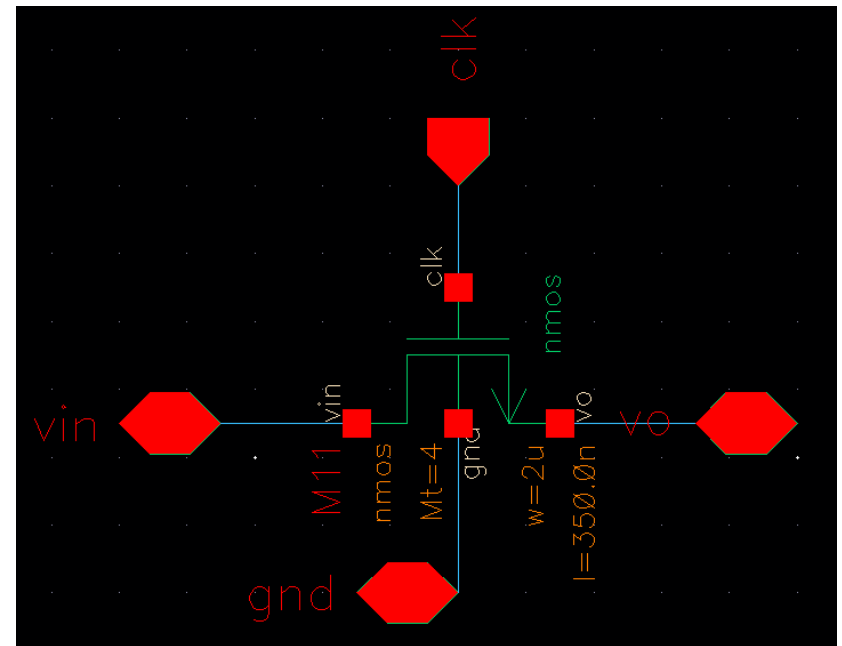


3-bit SAR ADC

■ sw0,

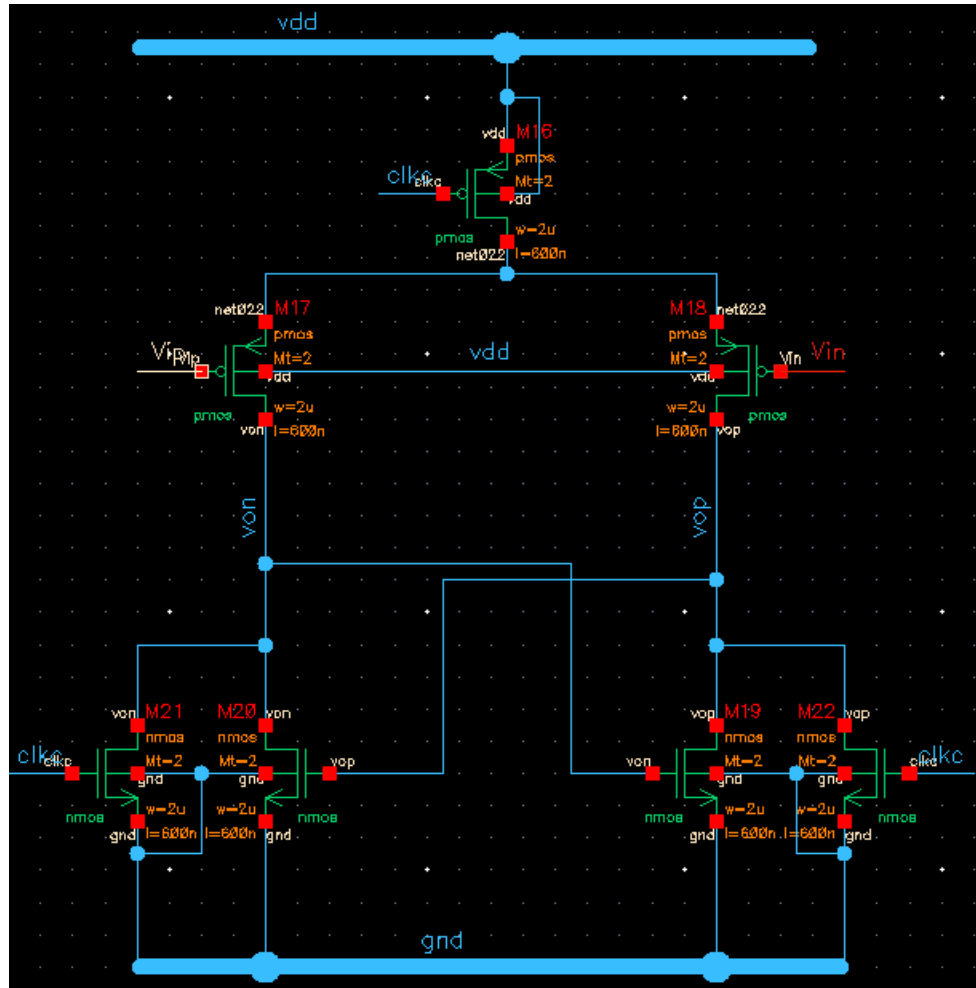


swVR



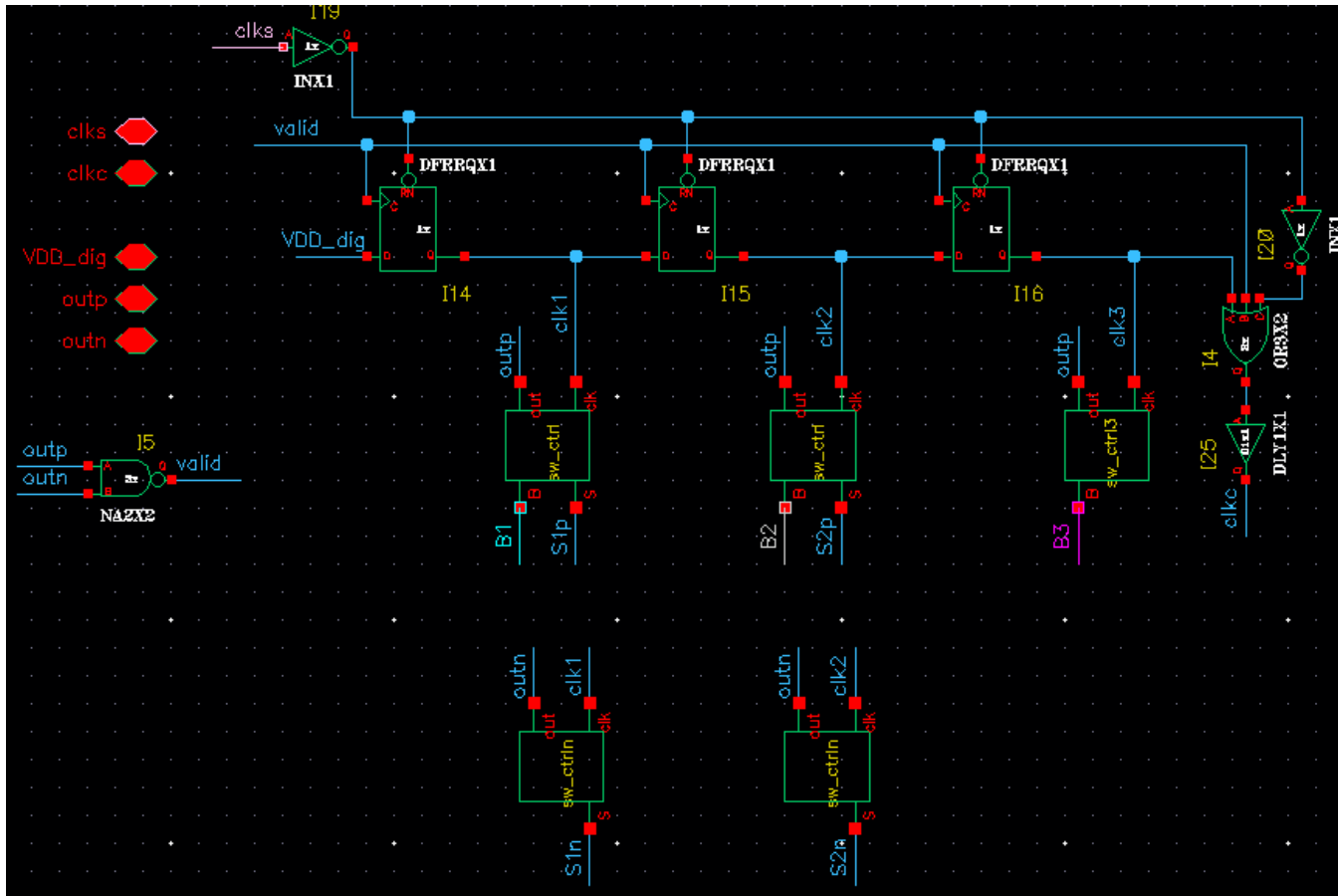
3-bit SAR ADC

■ Comparator



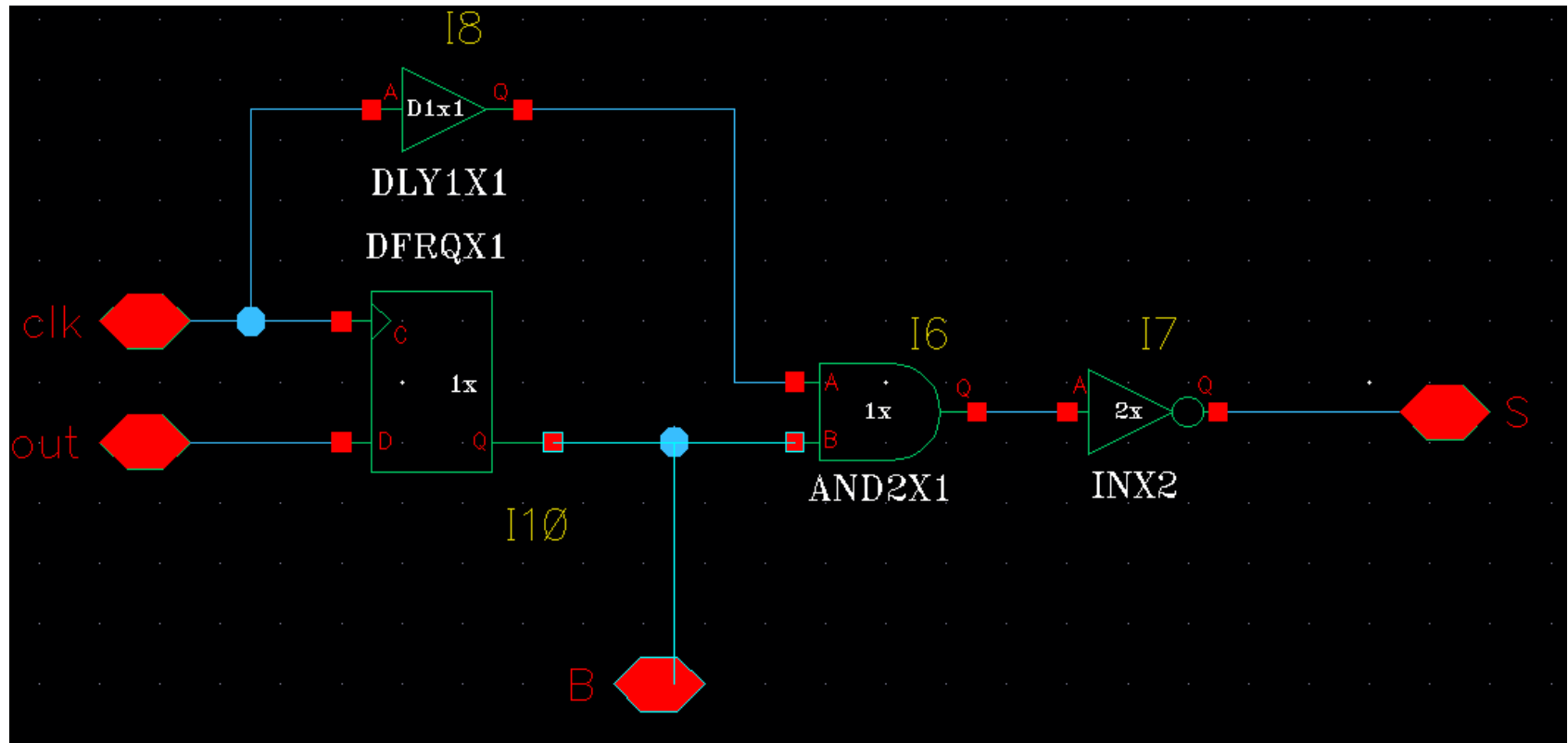
3-bit SAR ADC

- SAR logic — INX, NAND, OR, DFF, sw_ctrl, sw_ctrl3, sw_ctrln



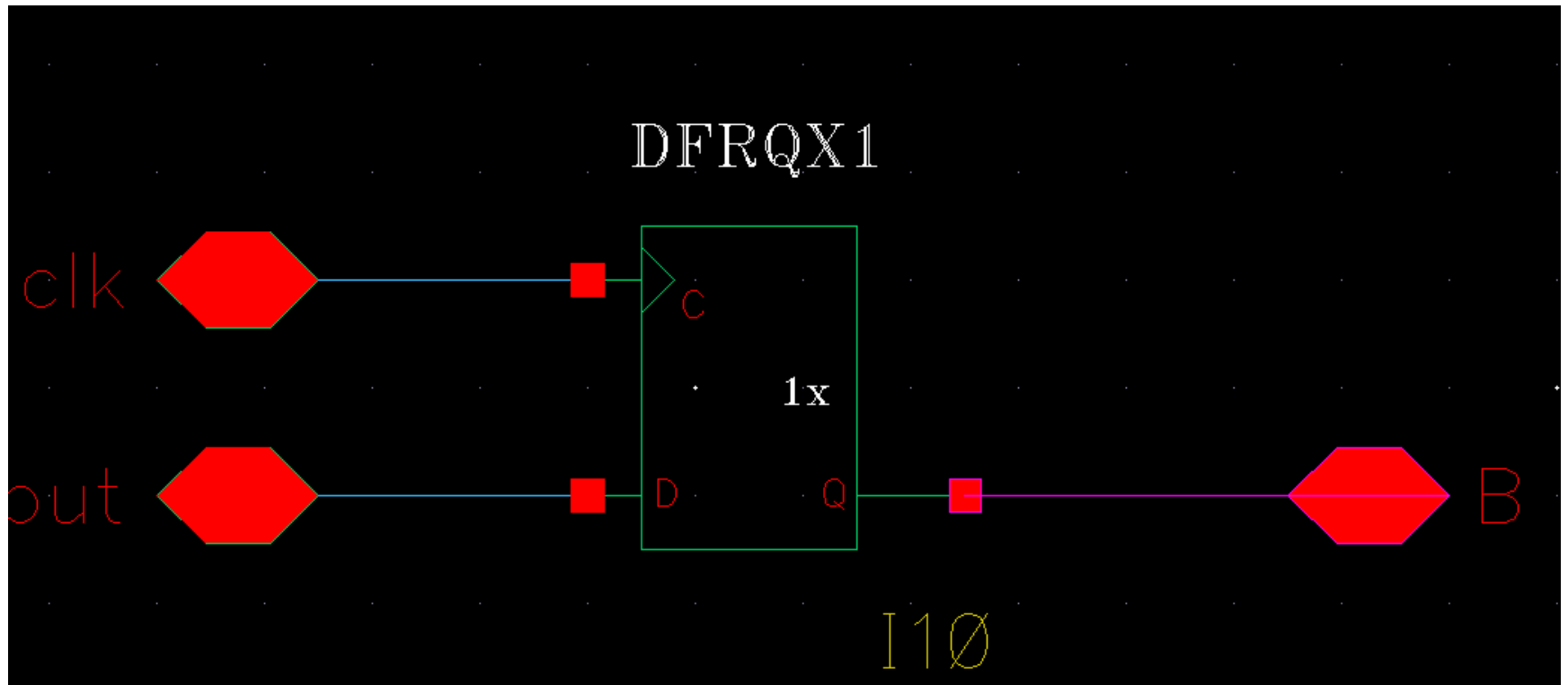
3-bit SAR ADC

■ sw_ctrl



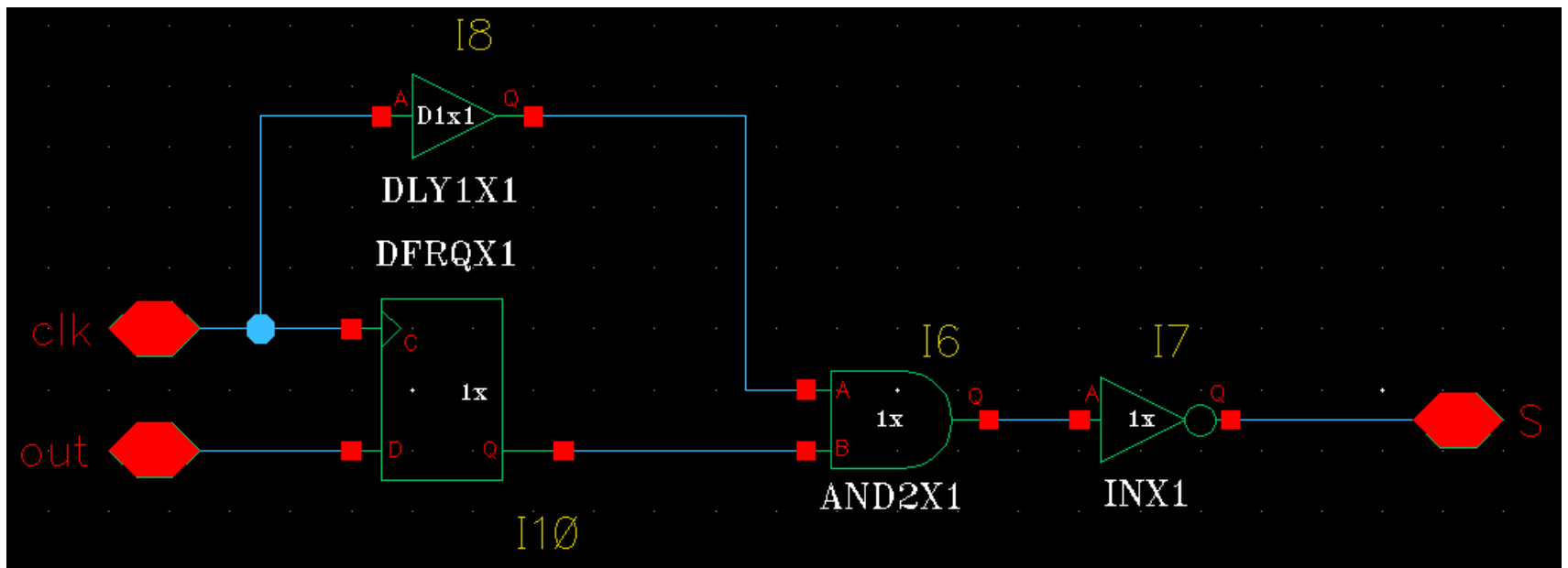
3-bit SAR ADC

■ sw_ctrl3



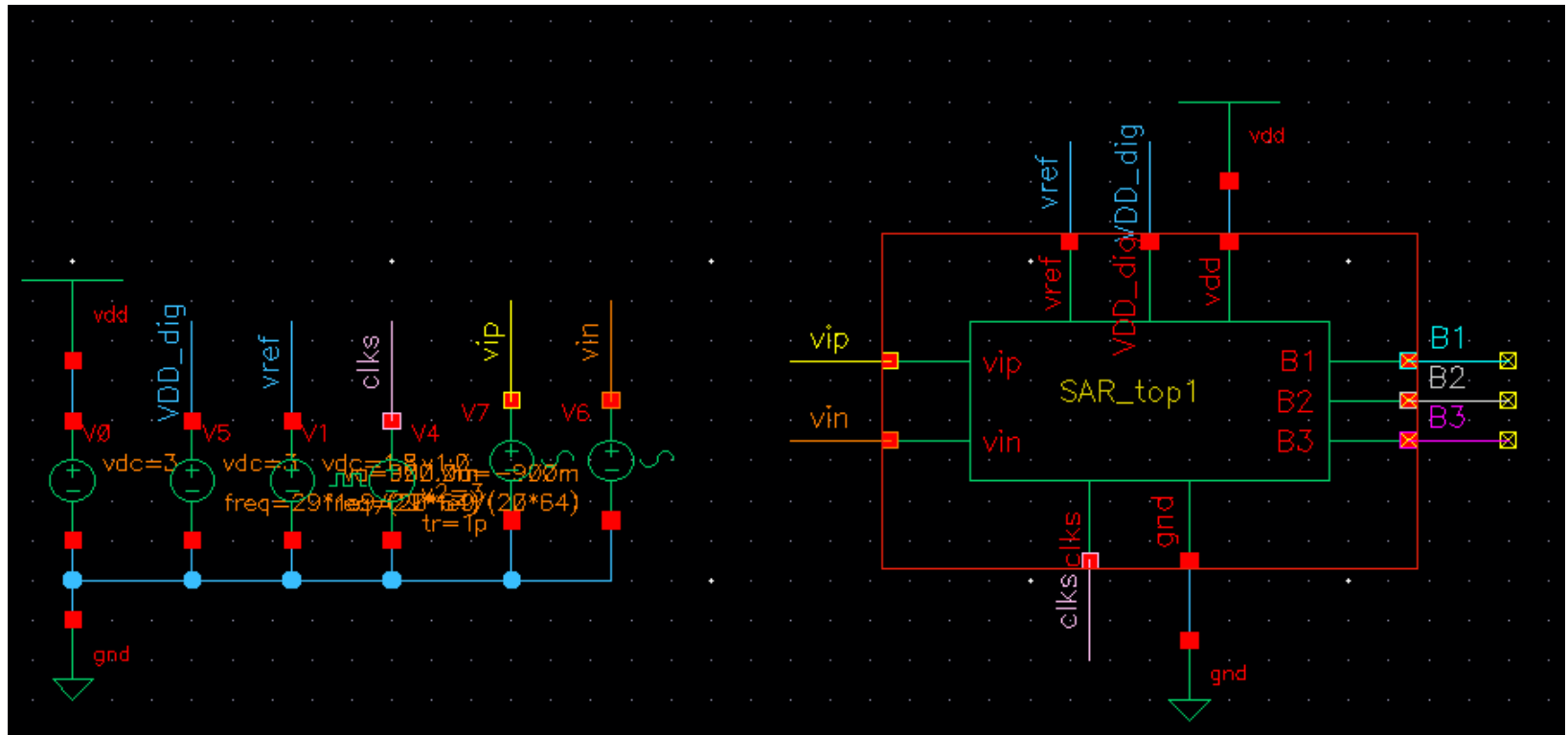
3-bit SAR ADC

■ sw_ctrlIn



3-bit SAR ADC

■ Testbench



Vdd=3V, VDD_dig=3V, vref=1.8V

3-bit SAR ADC

■ Testbench

Voltage 1	0 V
Voltage 2	3 V
Period	20n s
Delay time	2n s
Rise time	1p s
Fall time	1p s
Pulse width	8n s

clks

DC voltage	900.0m V
AC magnitude	
AC phase	
XF magnitude	
PAC magnitude	
PAC phase	
Delay time	0 s
Offset voltage	
Amplitude	900.0m V
Initial phase for Sinusoid	
Frequency	29*1e9/(20*64) Hz

vip

DC voltage	900.0m V
AC magnitude	
AC phase	
XF magnitude	
PAC magnitude	
PAC phase	
Delay time	0 s
Offset voltage	
Amplitude	-900m V
Initial phase for Sinusoid	
Frequency	29*1e9/(20*64) Hz

vin

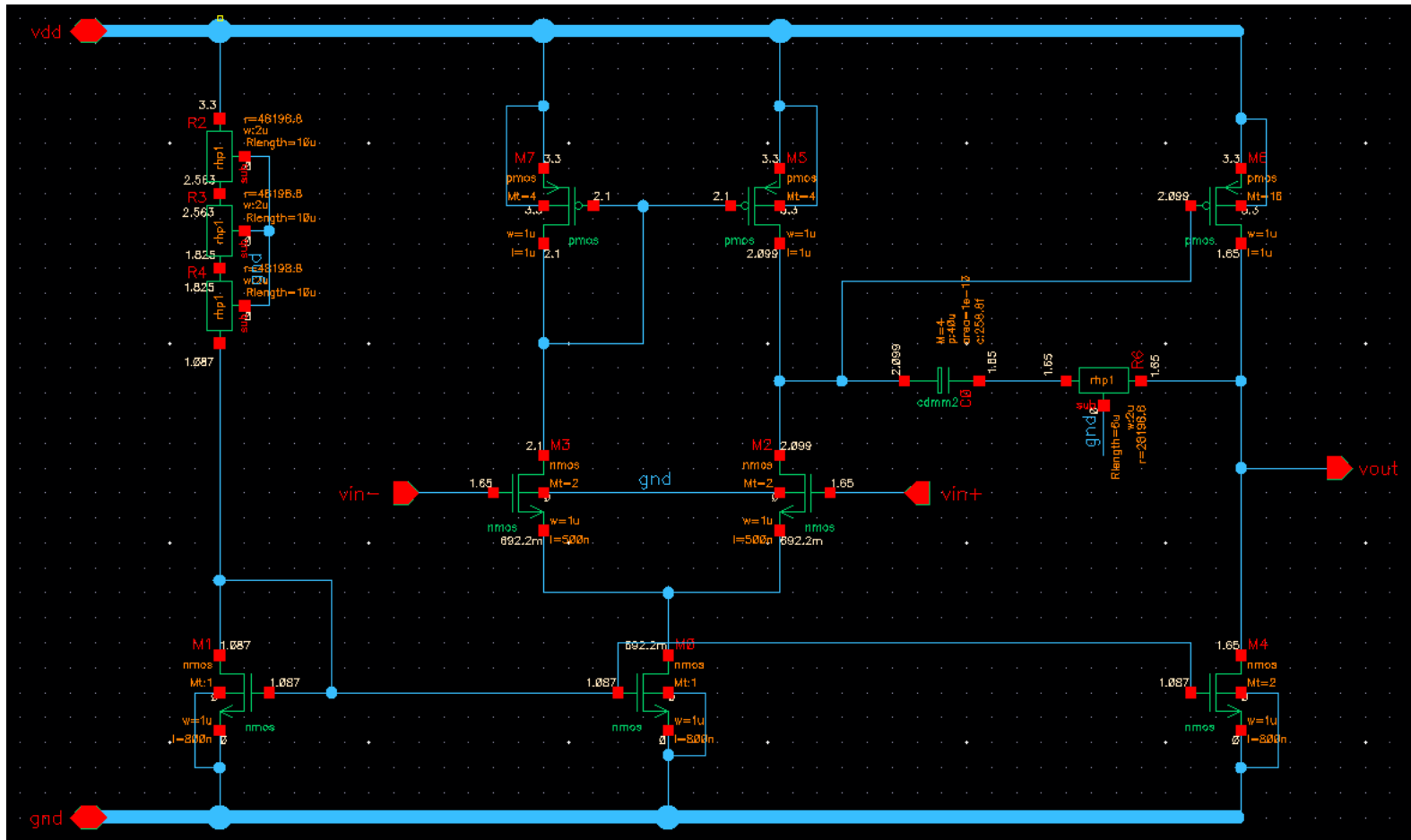
3-bit SAR ADC

■ Your task

- Draw the schematic of SAR ADC
- Do tran pre-simulation and calculate SNDR
- Draw the layout
- Do tran post-simulation and calculate SNDR
- Compare the results and discuss carefully

2-stage OPA

■ Structure of OPA



2-stage OPA

- Structure of OPA

- Resistor:

Resistance	48198.8 Ohms
Width	2u M
Length	10u M
Multiplier	1

Rhp1 for bias

Resistance	28198.8 Ohms
Width	2u M
Length	6u M
Multiplier	3

Rhp1 for miller compensation

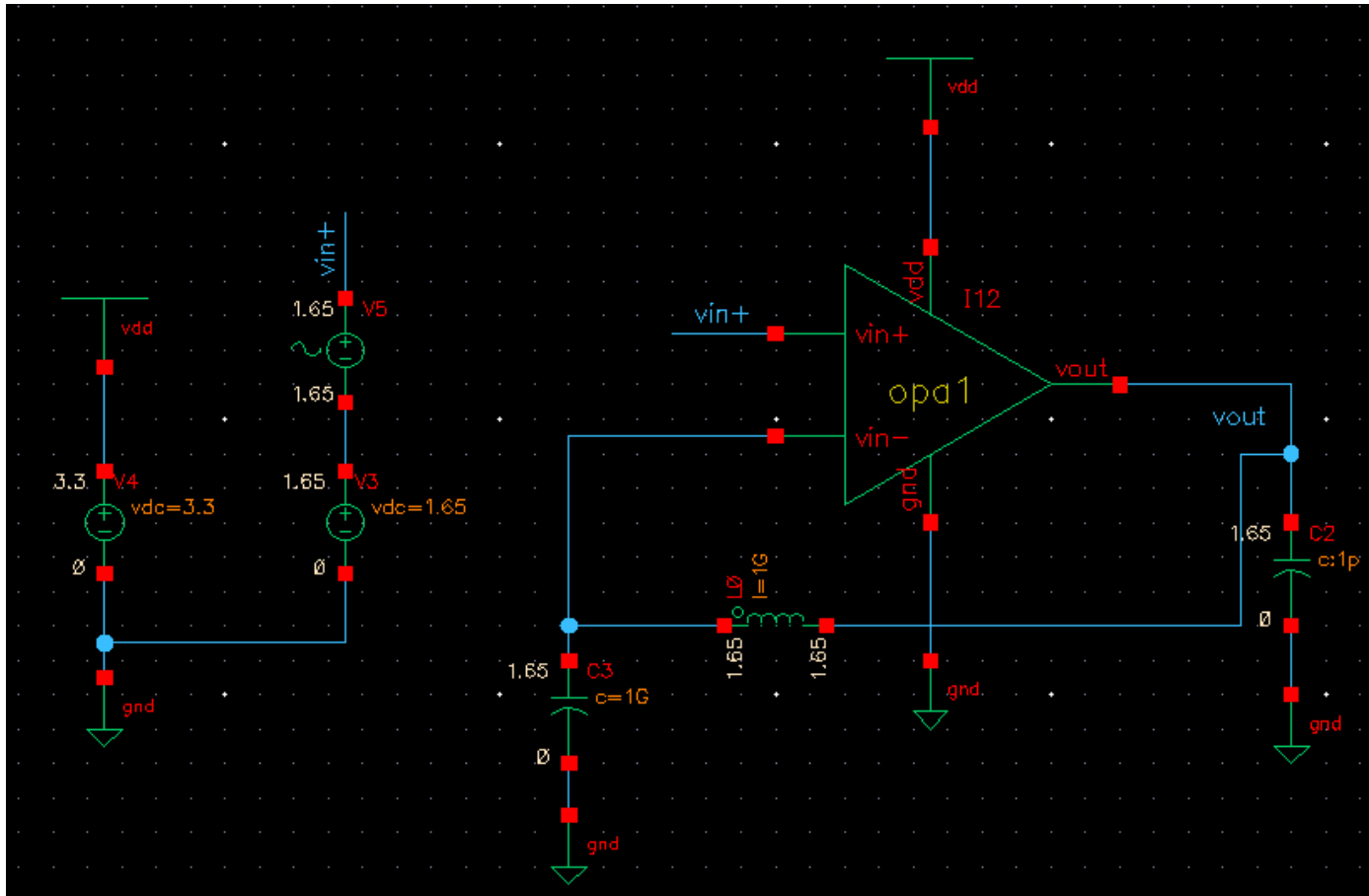
- Capacitor:

Unit Capacitance	258.8f F
Width	10u M
Length	10u M
Multiplier	4

cdmm2

2-stage OPA

- Testbench



2-stage OPA

■ Your task

- Draw the schematic of OPA
- Do pre-simulation and calculate DC gain, PM, GBW (in different PVTs)
- Do monte-carlo pre-simulation
- Draw the layout
- Do post-simulation and calculate DC gain, PM, GBW (in different PVTs)
- Do monte-carlo post-simulation
- Compare the results and discuss carefully



Thanks!

